Ph. D. DISSERTATION

Analysis of NBTI Reliability and Comparison in 3D MOSFET Devices and Parasitic Resistance Modeling

3D MOSFET 소자에서의 NBTI 신뢰성 분석 및 소자 비교와 기생 저항 모델링

BY

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ABSTRACT

CMOS devices have enabled sustainable scaling by changing its structure from planar MOSFETs to 3D multi-gate MOSFETs. However, a gate electric field is increased as the device size and oxide thickness are scaled down. The increased gate electric field increases the mobile carrier concentration in the channel and source/drain. Thus, this severely degrades the device reliability which causes issues such as negative bias temperature instability (NBTI), and also affects the parasitic resistance. In this thesis, the inherent characteristics of various 3D MOSFET devices are firstly compared focusing on the same condition of the parasitic components. Secondly, NBTI characteristics are investigated by changing the gate electric field and temperature conditions in 3D MOSFETs. The parasitic resistance of the extension region is newly modeled by considering the gate fringing field that varies depending on the spacer material type.

The 3D MOSFET characteristics of nanowire-FETs, nanoplate-FETs (NPFETs), and FinFETs were intrinsically compared at the same areas in the metal gate and silicon channel by focusing on the same parasitic components. Since the NPFET structure has the highest effective channel width among other structures, which not only enhances the delay performance, but also improves immunity to short-channel effects. In addition, it is found that the use of a dual-k spacer with the NPFET further improves the on-state performance and could be an important solution for future next-generation devices.

In the case of NBTI, the change of V_T depending on the gate voltage and temperature is firstly calibrated based on 10-nm node FinFET measurement. In addition, the NBTI Reaction-Diffusion model is newly remodeled by considering the scattering rate which is dependent on the temperature. Additionally, trap components are extracted from

experimental data of 10-nm node FinFETs, which indicate that the proper stress gate voltage (V_{GSTR}) is required in order to appropriately predict the device end-of-life time. Furthermore, it is found that not only the V_{GSTR}, but the gate work-function (WF) is also a significant factor that determines the NBTI characteristics. Based on the calibrated framework model, the NBTI characteristics of NPFETs are also studied and it is shown that that structure parameters such as channel thickness and width have significant effects on the NBTI characteristics.

A new model for parasitic extension resistance is also proposed considering the effect of the spacer dielectric constant. As the spacer material is changed from low dielectric constant materials to high dielectric constant materials, more carriers are accumulated at the surface of the extension region due to the gate fringing field. The model shown in the previous study only presents the accumulated carriers by using the fitting parameter of flat-band voltage (V_{FB}), but this model does not accurately reflect physical phenomena. The newly proposed model is developed based on the extension surface potential, which is dependent on the spacer dielectric constant. Considering this surface potential, not only the accumulated carriers, but the carrier mobility is also redefined and the accuracy of the new resistance model is validated by changing physical parameters such as doping concentration, spacer materials, width, and thickness.

Keywords: 3D FET, FinFET, Nanoplate-FET (NPFET), Negative Bias Temperature Instability (NBTI), Spacer, Parasitic Resistance

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Chapter 1
Introduction

1.1 3D MOSFETs Device

FinFETs have successfully enabled continuous scaling down from planar bulk MOSFETs by not only enhancing device performance, but also improving the gate controllability of the channel at reduced channel length. As FinFETs has three-dimensional (3D) multi-gates wrapped around the channel on three sides, the effective channel width and gate capacitance are greatly increased. For further scaling down, the process technology to make taller and narrower Fin is inevitably needed. However, FinFETs are facing many challenges such as patterning, performance, and layout issues as shown in Fig. 1.

Recently, a complementary-FET (CFET) architecture has been proposed [2,3]. This architecture includes a PMOS and NMOS structure built on top of each other instead of them structured side by side, as shown in Fig. 2. Although, the CFET has a strong point that it overcomes the inherent real estate limitation by increasing device density, many challenges remain such as the metal recess process step, buried metal rail process step, and parasitic resistance issues. In order for mass production, the tremendous process technology that can solve these problems must be developed.

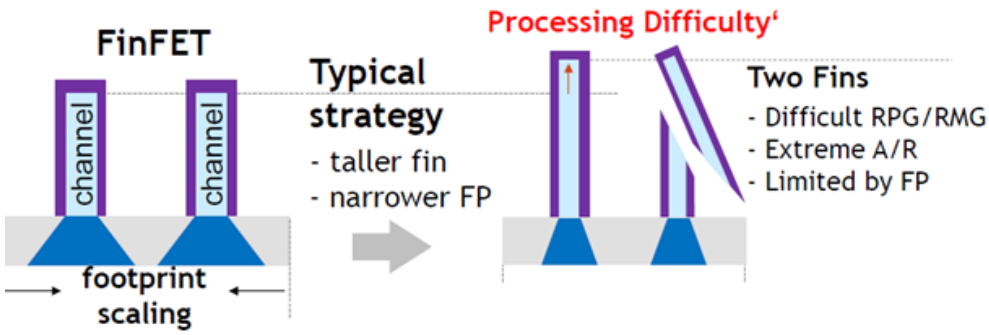

Fig. 1. Challenges for FinFET for further scaling down [1].

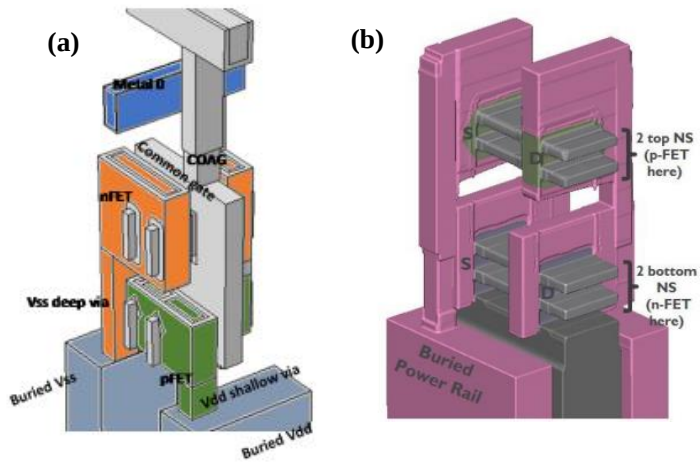

Fig. 2. 3D view of Complementary FET of (a) FinFET (b) nanoplate-FET [2,3].

In a recent, a more robust structure such as gate-all-around (GAA) nanowire-FETs (NWs) and nanoplate-FETs (NPFETs) are likely to become a potential candidate to replace conventional FinFETs due to its high improvement of device performance with sub-5 nm technology (refer to Fig. 3). This is because they effectively control short channel effects (SCEs), as well as improve the device performance in contrast to FinFETs (refer to Fig. 4).

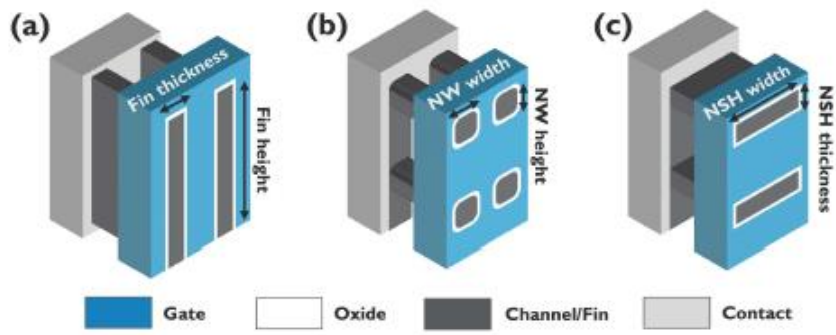

Fig. 3. 3D view of (a) FinFET, (b) nanowire-FET, and (c) nanoplate-FET [4].

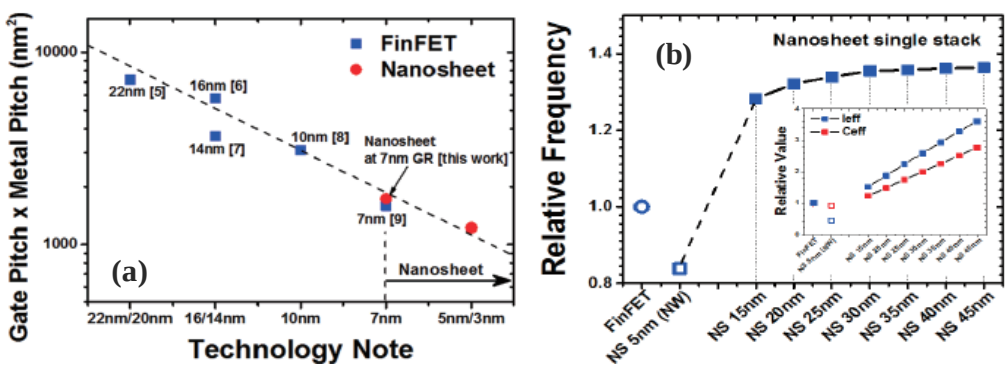

Fig. 4. (a) Overall area according to the technology node, (b) Relative outstanding device performance of NPFETs compared to FinFET [5].

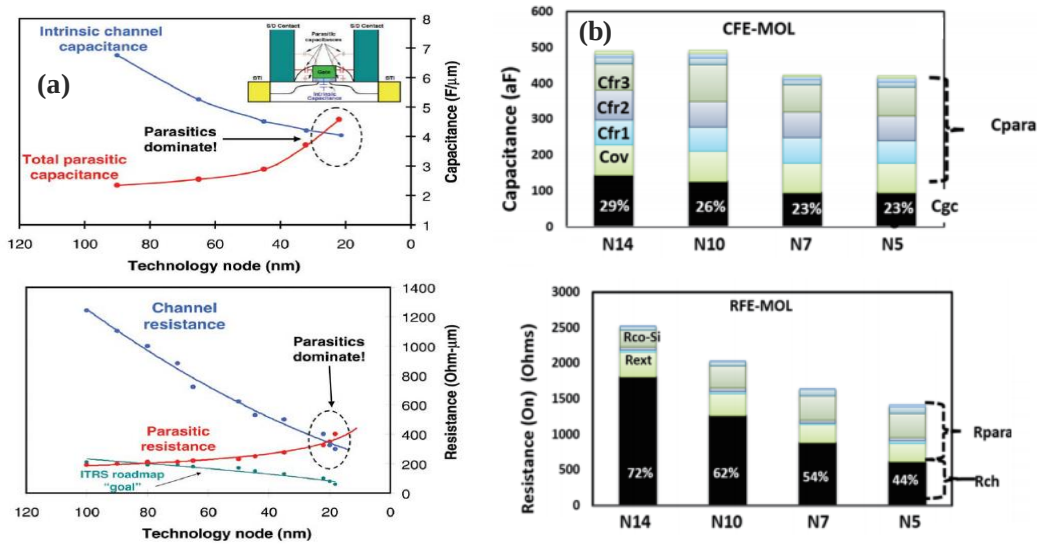

Fig. 5. Electric field according to technology node from [6,7].

Parasitic resistances and parasitic capacitances have been regarded as crucial factors since they greatly exacerbate device performance (in Fig. 4). To be specific, sub-10 nm technology node, the overall parasitic resistance portion to the channel greatly increases as shown in Fig.4. Thus, the parasitic components are no more negligible. However, the previous study only shows the outstanding performance of NPFETs in contrast to FinFETs in a given footprint, as shown in Fig. 2. In this case, the parasitic components have different values due to the different silicon channel areas, which have significantly different effects on the device performance. Thus, investigation on a fundamental comparison is desperately required based on the same condition of parasitic components with different channel shapes (Fin, NW, and NP).

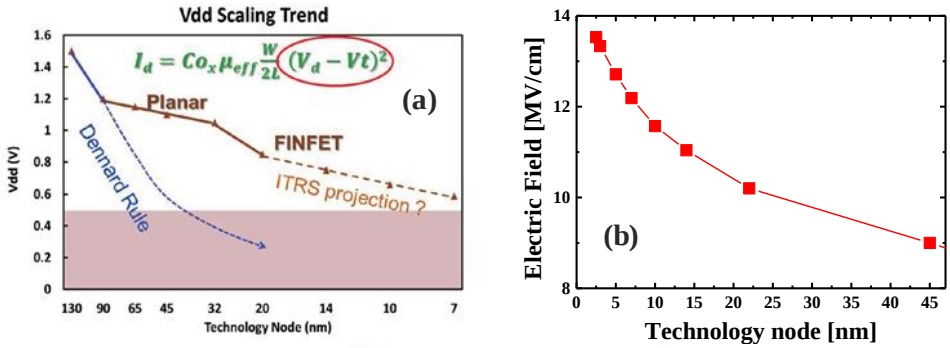

Fig. 6. Electric field according to technology node from [8,9].

In addition, the gate electric field is increased with aggressive scaling down of the oxide thickness. To make matters worse, the supply voltage (V_{DD}) scaling down is quite difficult. This is because the reduction of V_T causes problems such as the leakage currents, SCEs and random dopant fluctuation [8]. Thus, this increased gate electric field unexpectedly increases the mobile carriers in the parasitic resistance region. Thus, a precise parasitic resistance model, which fully reflects the gate field effect at one-digit nanometer technology nodes, is inevitably needed for device design. In addition to parasitic resistance model, the increased gate electric field severely degrades the reliability issues such as bias temperature instability (BTI) due to the generated traps between gate insulator and silicon channel. Thus, the study of BTI is considered very important for further scaling down.

1.2 What is Negative Bias Temperature Instability (NBTI)?

Bias temperature instability (BTI) has been regarded as a serious reliability concern since it continually threatens the performance and lifetime of complementary MOS (CMOS) devices and circuits. Fig. 3 shows the CMOS inverter operation and most biases are related to BTI. As device size and gate thickness are aggressively scaled down to sub-5 nm technology, the oxide electric field governing BTI degradation increases. The supply voltage is not scaled to the extent of the same factor as device dimension is scaled down, which accordingly worsens reliability. Thus, device parameters including threshold voltage shift (V_T), drain current (I_{DS}), subthreshold slope (S.S.), and transconductance (g_m) become increasingly vulnerable to BTI. Thus, the investigation of BTI characteristics is regarded as the most important factor in the reliability of modern devices.

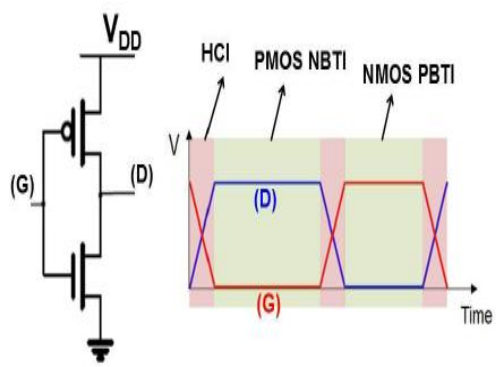

Fig. 4. CMOS inverter circuit and its bias operation [10]

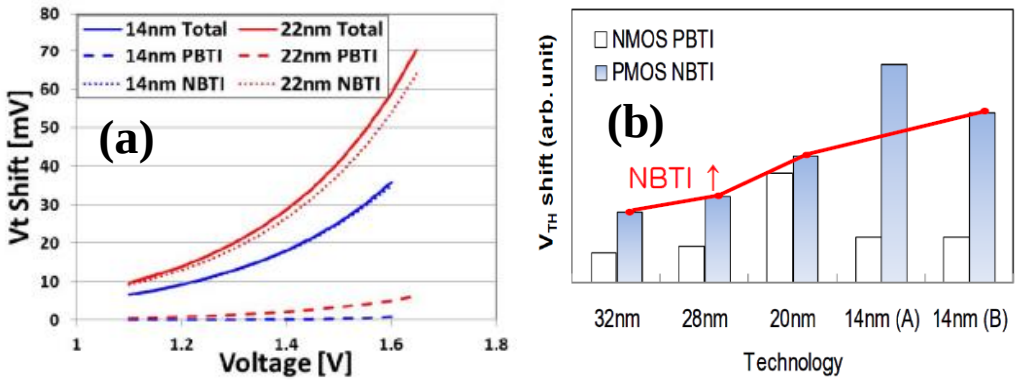

Fig. 5. BTI characteristics according to the (a) stress voltage and (b) technology nodes [11,12].

Negative bias temperature instability (NBTI) in PMOS and positive bias temperature instability (PBTI) in NMOS mechanisms coexist in CMOS inverter circuit operation. NMOS PBTI is related to the electron trapping in high-*k* bulk oxide and PMOS NBTI degradation occurs in the interlayer oxide. As the oxide thickness is scaled down to reduce the bulk-trap volume and metal workfunction is tuned to reduce electric fields, NMOS PBTI becomes nearly negligible in sub-22 nm nodes (Fig. 4). However, scaling down of the interlayer is much more challenging since it is typically in the range of 0.6 ~ 0.8 nm [12]. In addition, the poor quality of the interlayer with increased E-field further degrades the NBTI. Thus, it is very important to investigate the NBTI characteristics in modern devices.

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Chapter 2

Comparison of 3D FETs with Spacer Materials

2.1 Introduction

FinFETs have enabled sustainable scaling from planar MOSFETs by alleviating the short channel effects (SCE). However, as this aggressive scaling is being undertaken with sub-10-nm technology nodes, a more robust structure is required to completely control the SCE. Thus, not only the GAA nanowire-FETs(NW) but also GAA nanoplate-FET(NP) has become a likely candidate to replace FinFET [1–3]. In addition to the SCE, the parasitic resistance and capacitance have been regarded as being crucial factors since they greatly exacerbate the device performance [4,5]. From this perspective, previous studies [1,6] assumed that an NP achieves a higher level of circuit performance than any other structure for a given footprint. This is because NP offers a wider channel area by vertically stacking the channels in the same metal-gate area. However, in this case, the parasitic components have different values due to the silicon channel areas being different, which have clearly different effects on the device performance. In the present study, a fundamental comparison based on the silicon channel shapes (Fin, NW, and NP) was undertaken, focusing on the conditions of the parasitic components. The comparison was

conducted by considering not only the same footprint of the metal gate but also the same area of the silicon channel. Thus, each parasitic constituent has not only the same area but also the same length or thickness, regardless of the silicon shape. The parasitic components related to the spacer and extension region are known to constitute most of the parasitic components and have a predominant effect on the device performance of a sub-5-nm node [6–8]. Based on the exact calculation for the same areas, a fundamental comparison of the silicon channel shape was conducted. This comparison is only possible using a technology computer-aided design (TCAD) simulation. The device characteristics depending on the silicon structure shapes are analyzed in terms of the different aspects such as the parasitic components, the on- and off-state characteristics, and the delay properties. In addition, with the use of different spacer materials, the dual-*k* spacer for NP is investigated with the goal of taking further steps to improve all the device performances.

This paper is organized as follows. Section 3.2.1 presents the simulation setup for a 5-nm-technology node, while Section 3.2.2 shows the results of comparing NW, NP, and FinFET in terms of the various aspects. The investigation for the dual- and single-*k* spacers is shown in Section 3.3. Finally, a summary of the findings of the present study is presented in Section 3.4.

2.2 Comparison of 3D FETs Device Structure

2.2.1 Simulation & Device setup

To compare the structures, 3D technology computer-aided design (TCAD) simulation was used. In terms of the simulation accuracy, the calibration was conducted for the drain current of a 3-stack NP of a sub-5-nm-technology node addressed in a previous study [1], as shown in Fig. 1(a). A 5-nm layer and 5-nm spacer thickness are assumed for the simulation with the benchmark of [1,6]. This is because the 5-nm layer of NP could be fabricated with the available techniques and offers superior electrostatic control [1, 6]. The supply voltage (V_{DD}) was set to 0.65 V and the metal thickness (T_M) was fixed to 5 nm considering that the fabricated NPFET had a sheet-to-sheet thickness of 10 nm. The other physical parameters are listed in Table 1. To fundamentally compare the device characteristics according to the silicon shape, only a single channel was used for NMOS. Figure 2 shows the simulated structures of the NW, NP, and FinFET, while Fig. 3 shows a cross-sectional view of the silicon channel having the same silicon area for each structure. Assuming that NW has a completely circular channel, the diameter of NW(T_{NW}) is changed from 3 to 10 nm. The thickness of NP (T_{NP}) and Fin (T_{Fin}) is fixed to 5 nm to compare each under the same carrier mobility conditions, given that the electron mobility is directly related to the thickness of the layer. However, the width of NP (W_{NP}) and the height of Fin (H_{Fin}) is changed as T_{NW} is altered in order to attain the

same area of not only the silicon channel (or the source/drain(S/D) extension) but also the gate metal (metal height × metal width in Fig. 3). Since the areas of the silicon and metal gate have a direct relationship with the parasitic resistance and capacitance, greatly degrading the device delay performance, all of the comparisons for different structures were conducted using the same areas.

TABLE I
DEVICE PARAMETERS IN [10]

Device Parameter		**Device Parameter**	
Channel Length (L_{CH})	10 nm	Contact Resistivity	3E-9 $\Omega \cdot cm^2$
Gate Length (L_G)	12 nm	V_{DD}	0.65 V
Spacer Length (L_{SP})	5 nm	Effective Oxide Thickness	0.75 nm (HfO_2 / SiO_2 : 1.5 / 0.5 nm)
Source/Drain Doping	10^{21} cm^{-3}	Spacer Dielectric	1, 3.9, 7.5, 22
Channel Doping	10^{16} cm^{-3}	T_{NW}	3 ~ 10 nm
T_M	5 nm	Contacted Poly Pitch	44 nm

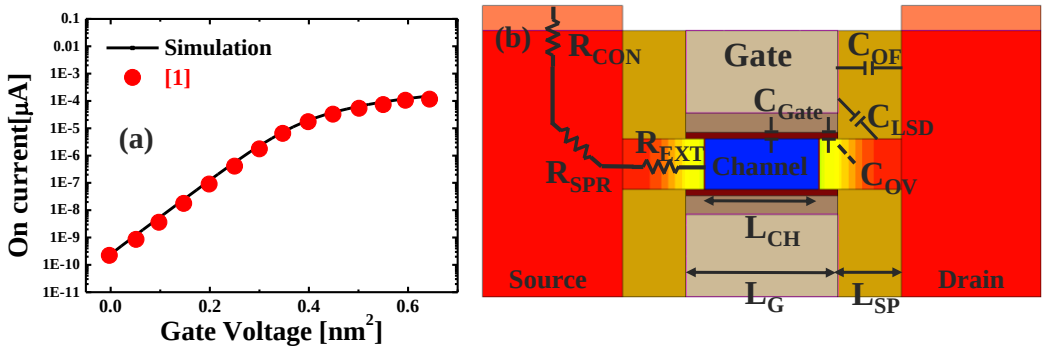

Fig. 1. (a) Calibration for the drain current of [1] (b) Cross section view of NP FET and each parasitic component of resistances and capacitances

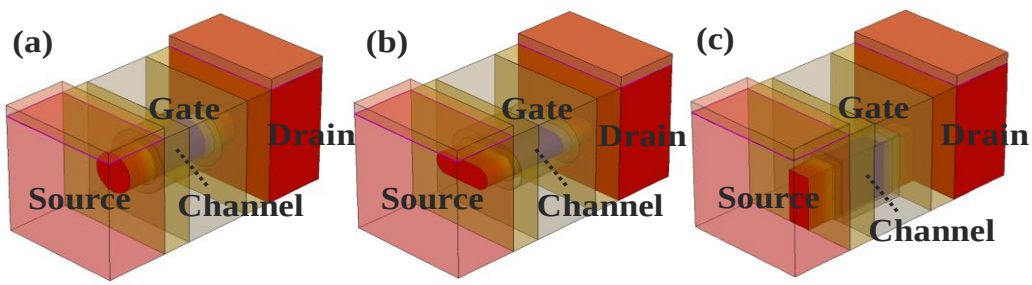

Fig. 2. (a) Calibration for the drain current of [1] (b) Cross section view of NP FET and each parasitic component of resistances and capacitances

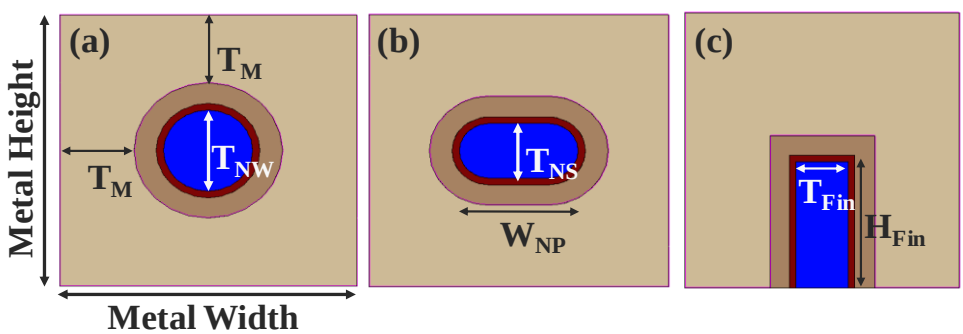

Fig. 3. Cross section view of single (a) NW FET (b) NP FET (c) Fin FET.

The electron mobility is degraded as the thickness of the silicon is decreased [9–12] but the electrons form a volume inversion at the center of the channel which reduces the surface roughness scattering when the Si channel width is a few nanometers [13,14]. Thus, Lombardi's the thin-layer mobility model is used because it considers geometric quantization effects on the mobility at a thickness of a few nanometers, such as thickness fluctuation scattering, surface roughness, and phonon scattering. [15]. The density gradient model is also used to describe quantization effects and the hydrodynamic model is applied for the simulation, considering the temperature of the carrier and lattice [16]. The other physical parameters are calibrated to satisfy the International Technology Roadmap for Semiconductors (ITRS) for the 5-nm-technology nodes [17]. As shown in Fig. 1(b), the parasitic resistance components are connected in series with the contact resistance (Rcon) between the metal and bulk S/D, the extension resistance (R_{EXT}) between channel and S/D bulk, and the spreading resistance (R_{SPR}) where the current spreading phenomenon has occurred. Also, the parasitic capacitances are also connected in parallel from the gate to the S/D with the direct outer-fringing capacitance (C_{OF}) between the gate to S/D bulk, the fringing capacitance from the metal to the low S/D doping region (C_{LSD}), and the overlap capacitance (C_{OV}), shown in Fig. 1(b). Assuming the use of state-of-the-art CMOS technology, the contact resistance per area was fixed to $3 \times 10^{-9}\ \Omega \cdot cm^2$ [18]. To adjust the requisite threshold voltage(V_T) to 205 mV, the gate metal work function is also changed depending on the effective channel width for the different structures. (I_{VT} = 100 nA × (W/L)).

2.2.2 Comparison of Device Structure

Equations (1)–(3) express the silicon channel area of each structure (NP, NW, and Fin) while Eq. (4)–(6) shows the effective channel width of each structure. Since all of the silicon channel area has the same area as the silicon channel, the effective channel width of each can be expressed by T_{NW} as shown given by Eqs. (4)–(6). Figure 4(a) also shows the effective channel width of each structure along the silicon area.

$$A_{NW} = \pi(T_{NW}/2)^2 \tag{1}$$

$$A_{Fin} = H_{Fin} \times T_{Fin} \tag{2}$$

$$A_{NP} = \pi(T_{NP}/2)^2 + T_{NP}(W_{NP} - T_{NP}) \tag{3}$$

$$W_{Eff,NW} = \pi T_{NW} \tag{4}$$

$$W_{Eff,Fin} = T_{Fin} + 2H_{FIN} = \pi\left(\frac{T_{Fin}}{\pi} + \frac{T_{NW}^2}{2T_{Fin}}\right) \tag{5}$$

$$W_{Eff,NP} = \pi T_{NP} + 2(W_{NP} - T_{NP}) = \pi\left(\frac{T_{NP}}{2} + \frac{T_{NW}^2}{2T_{NP}}\right) \tag{6}$$

From Eqs. (4)–(6), it is known that the NP structure effectively increases the channel width relative to other structures as T_{NW} is increased ($T_{NS} = T_{Fin} = 5$ nm). As shown in Fig. 4(a), as the silicon area is increased, the NP has the highest effective channel width. Thus, the NP has not only the highest on current ($V_{GS} = V_{DS} = V_{DD}$) in Fig. 4(c) but also the largest gate capacitance (Fig. 4(b)). The parasitic capacitance of C_{OF} (inset in Fig. 4(b)) is

almost the same regardless of the device structure, since the same area of C_{OF} is considered. The intrinsic gate delay is usually expressed by multiplying the total resistance and total capacitance in the on-state and corresponds to the minimum delay of the device itself [19]. Normally, there is an inverse relationship between the total capacitance and the total resistance with variations in the effective channel width. As the effective channel width is increased, it boosts not only the increment of the on-current (or the decrement of the resistance) but also the growth of the gate capacitance due to the direct relationship between the effective channel width and the gate capacitance area. In the case of NP, the on-current and gate capacitance exhibit an 80% growth rate with a change in the silicon area from 28 to 64 nm^2, but the total capacitance of the NP has only a 50% increase rate. Therefore, the intrinsic gate delay of NP exhibits a decreasing trend with an increase in the silicon area, while having the lowest delay characteristics due to its having the greatest effective channel width.

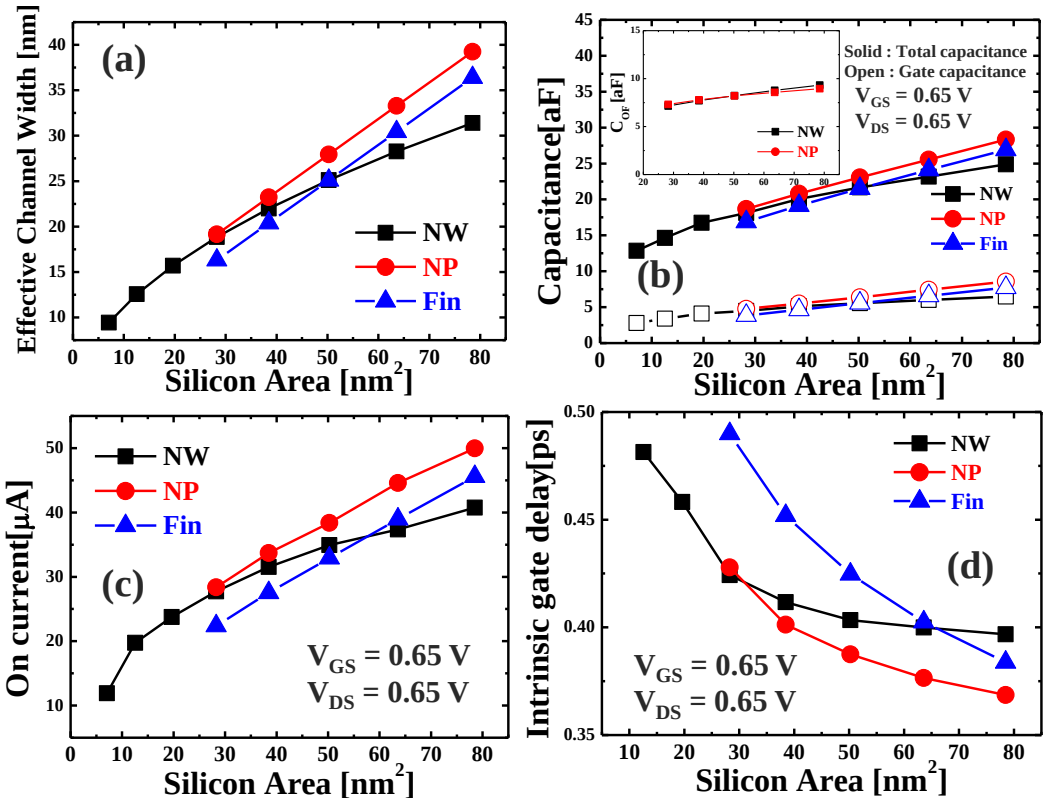

Fig. 4. (a) Effective channel width (b) Total capacitance (c) On current (d) Intrinsic gate delay according to the NW, NP, Fin structures.

Similar aspects are shown for the NMOS inverter delay (Fig. 5). The load capacitance is added to the output node (= 20 aF) considering the BEOL capacitance which is similar to the sum of the gate capacitance and parasitic capacitance of the FEOL and MOL capacitance [7,8]. Here, t_{PHL} is the NMOS inverter delay as the output voltage is dropped from V_{DD} to $0.5 \cdot V_{DD}$ and t_{Fall} is also a delay that arises as the output voltage is decreased from $0.9 \cdot V_{DD}$ to $0.1 \cdot V_{DD}$. The drive current becomes more crucial than the device capacitance due to the added output load capacitance. Thus, the NP also exhibits more minimum delay characteristics than any other structure, as shown in Fig. 5.

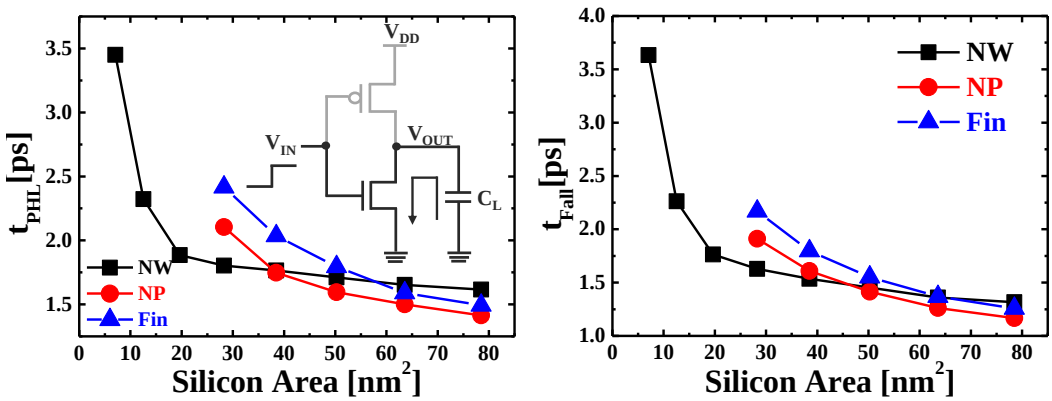

Fig. 5. (a) t_{PHL} and (b) t_{Fall} according to the NW, NP, Fin structures.

The off-state (V_{GS} = 0 V, V_{DS} = V_{DD}) characteristics are shown in Fig. 7. The drain-induced barrier lowering (DIBL) is measured at V_{GS} = 0 V, V_{DS} = V_{DD} and 0.05V. The sub-threshold swing (SS) is also measured in Fig. 7(d). All the off-state characteristics, such as the off current(I_{OFF}), DIBL, and SS exhibit similar trends with the effective channel width (Fig. 4(a)). Although, each structure of NP, NW, and Fin has the same area of silicon, the surface area of the channel (or the effective channel width) is different. Therefore, the gate capacitance of the NP effectively sustains the conduction band energy of the channel (Fig. 6) and it alleviates the effect of drain potential to a channel in the off-state. In short, due to the differences in the effective channel width, the NP exhibits not only better performance in the on-state but also stronger SCE immunity in the off-state.

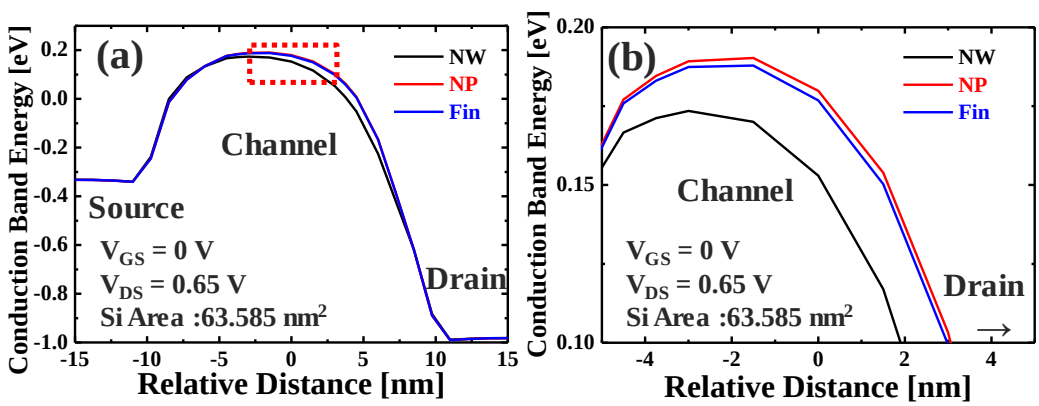

Fig. 6. Conduction band energy of NW, NP, and Fin structures at the center of the channel.

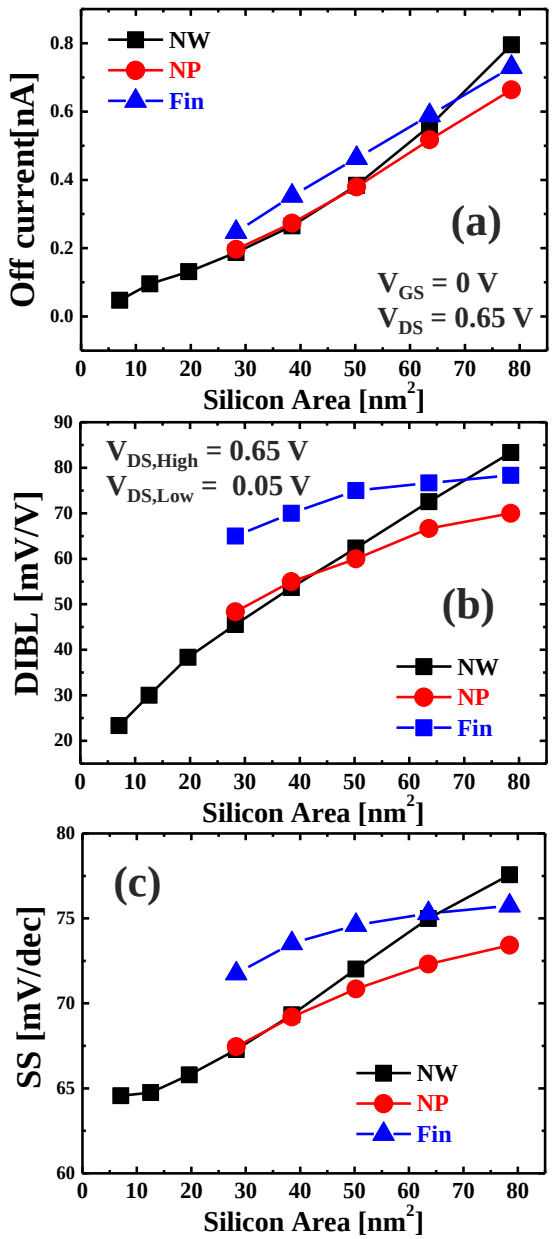

Fig. 7. (a) Off current (b) DIBL (c) SS according to the NW, NP, Fin structures.

2.3 Characteristics of the Various Spacer Materials

The parasitic components become more and more important as the device becomes smaller, especially in the case of a sub-5-nm technology node. Recently, spacer engineering has been regarded as being a compulsory technique for optimizing the delay characteristics of an NP structure since it has direct relationship with the on-current and capacitance [1, 20]. Thus, the parasitic components of resistance and capacitance are also extracted and compared with the NP structure, as shown in Fig. 8. The parasitic resistance of R_{CON} is the dominant factor determining the overall parasitic resistance but it depends on the Schottky barrier height and doping concentration at the interface between the metal and the semiconductor [18]. In addition to R_{CON}, not only R_{EXT} but also C_{OF} has a large portion of parasitic components.

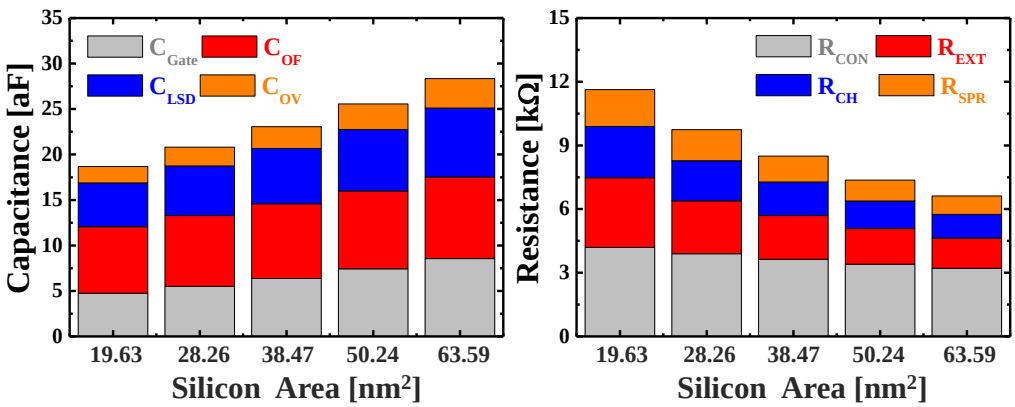

Fig. 8. Parasitic components of resistances and capacitance for NP structure.

It was known that using a high-*k* material to fabricate the spacer would cause the value of I_{ON} to increase. However, it also causes the overall parasitic capacitance to be elevated [21,22]. In case of a low-*k* material, it could reduce the parasitic capacitance but also decrease I_{ON} [23]. Recently, encased air-gap spacer structures have been experimentally investigated and have shown not only an enhanced delay performance but also a reduced parasitic capacitance [24]. As the air-gap spacer is enclosed by SiN material, it could be configured as a dual-*k* spacer which uses two different materials in the spacer region, as shown in Fig. 9. Given this trend, dual-*k* spacer engineering could be one the solutions since it not only decreases the parasitic capacitance of C_{OF} but also reduces the parasitic resistance of R_{EXT}. As a higher-*k* material is used adjacent to the gate metal (Fig. 9), a greater gate fringing field effect occurs which consequently boosts the on current [25-28]. In addition, the off-state characteristics (I_{OFF}, DIBL, SS_{AVG}, etc.) are also improved if a lower-*k* material is used [23]. Thus, the dual-*k* spacer is constructed as an encapsulated air spacer structure which consists of HfO_2 ($\varepsilon = 22$) and air ($\varepsilon = 1$) in this simulation

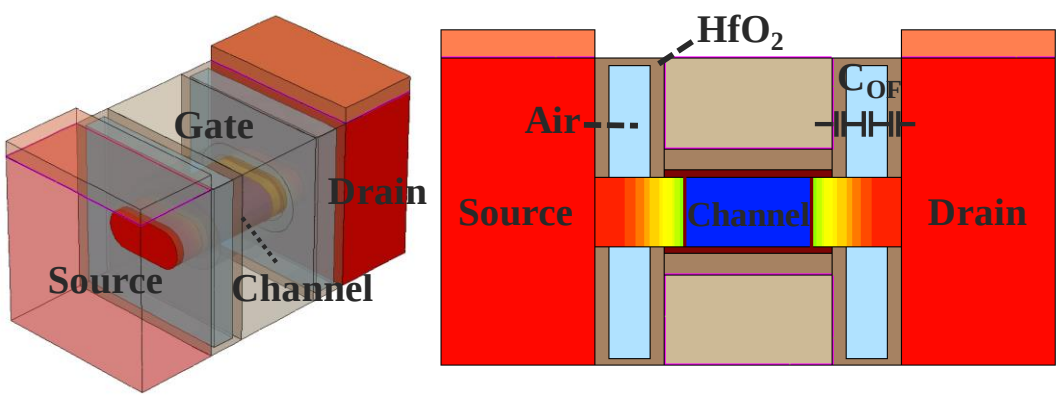

Fig. 9. 3D view and cross section view of the dual-*k* spacer structure for NP.

According to the extraction results for the parasitic components (Fig. 10), the dual-*k* (HfO_2/Air) spacer causes R_{EXT} to decrease with a similar level of single-*k* HfO_2 (use only one material in the spacer region) because a similar gate fringing field phenomenon occurs in the source/drain extension region. In addition, the parasitic constituent of C_{OF} also decreases due to the series connection of the different capacitance between the gate and the source/drain. Thus, the reduced R_{EXT} must increase I_{ON} and the decreased C_{OF} also make a contribution to the decrement of the total capacitance (Fig. 11). Therefore, with the increment of I_{ON} and the reduction of C_{Total}, the NMOS inverter delay characteristics (t_{PHL}, t_{Fall}) are more greatly improved than was previously observed for single-*k* Si_3N_4 (Fig. 12).

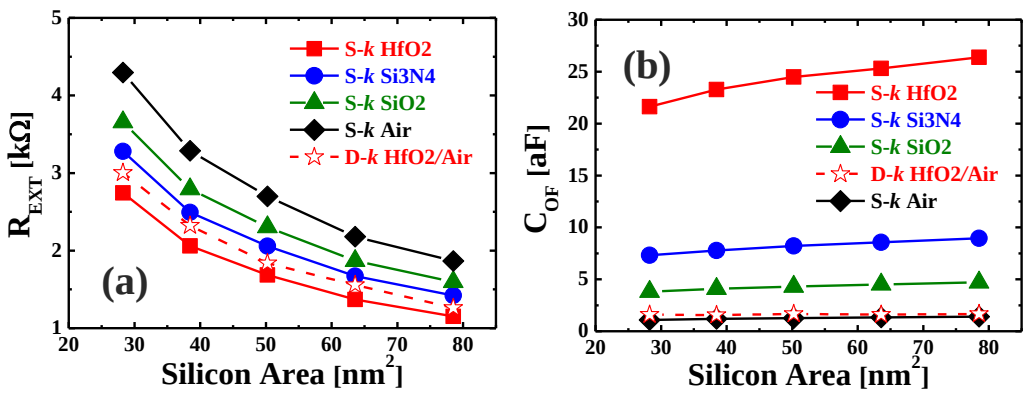

Fig. 10. Parasitic components of (a) R_{EXT} and (b) C_{OF}.

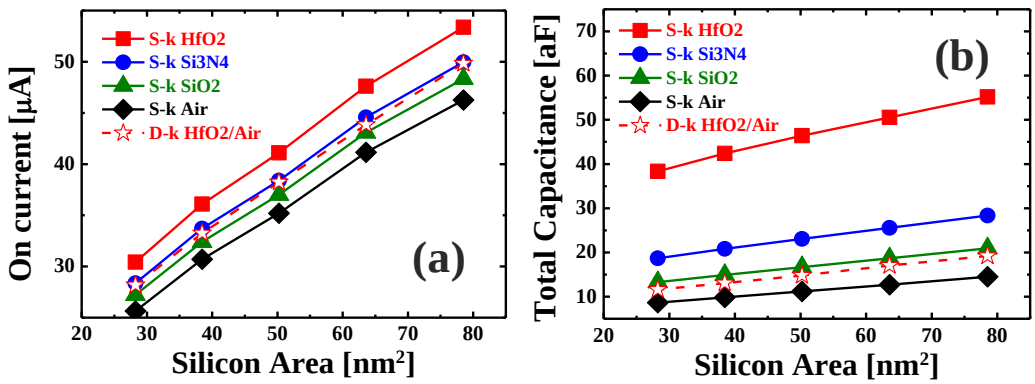

Fig. 11. (a) On-current and (b) Total capacitance with the use of different materials in the spacer.

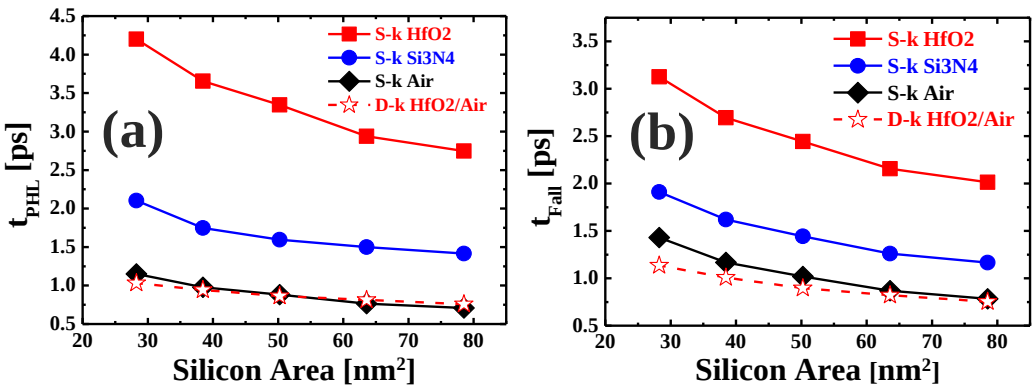

Fig. 12. (a) t_{PHL} and (b) t_{Fall} with the use of different materials in the spacer.

In addition to the improvement of the delay performances, the dual-*k* structure contributes to the progress of the SCE immunity. Figure 13 shows the off-state characteristics such as I_{OFF}, DIBL, SS_{AVG}, and I_{ON}/I_{OFF}. Unlike the single-*k* spacer, the dual-*k* spacer structure has two series-connected capacitances between the drain and extension regions. Thus, most of drain potential is dropped to the outer spacer capacitance and the drain potential has less effect on the channel. As a result, the dual-*k* spacer structure incurs lower values for I_{OFF}, DIBL, and SS_{AVG}. In terms of electrostatic control such as SS and DIBL, it is reasonable to use a device structure having a silicon area that approaches zero (Fig. 6). However, using the smaller silicon area reduces the on current, which causes the delay characteristics to be degraded, as shown in Figs. 4 and 5. Thus, the optimal point of the silicon area is still required considering not only the electrostatic control but also the delay performances. In this context, using the dual-*k* structure sub-5-nm technology node could act as a relaxation since it not only enhances the delay performance but also alleviates the short channel effects shown in Figs. 12 and 13. Thus, the use of a dual-*k* spacer could be a significant solution for future device generations.

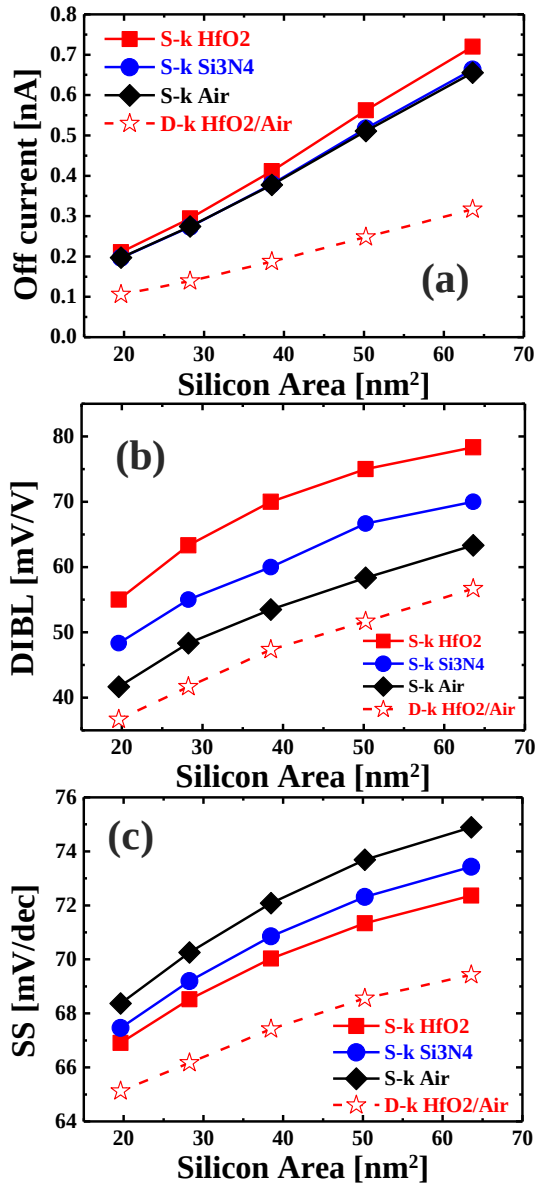

Fig. 13. (a) Off current (b) DIBL (c) SS using the different materials of the spacer region.

2.4 Summary

Comparing the NW, NP, and FinFET structures in the same area of a silicon channel, as well as the gate metal, reveals that the NP structure has the largest surface area of gate metal surrounding the channel. Thus, not only the on-state characteristics but also the off-state properties are greatly improved with the NP structure. In addition, the parasitic components of the resistance and capacitance are extremely relaxed as the dual-*k* spacer engineering is induced by the sub-5-nm node of the NP structure. As a result, it effectively enhances the delay performances.

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Chapter 3
Negative Bias Temperature Instability in 3D FETs

3.1 Introduction

Negative bias temperature instability (NBTI) is a significant reliability issue for p-type MOSFETs. As a device size is scaled down, the oxide electric field governing BTI degradation increases. The supply voltage is not scaled to the extent of the same factor of device dimension scaling, and thus the reliability concern worsens. Thus, device parameters including threshold voltage shift (V_T), drain current (I_{DS}), subthreshold slope (S.S.), and transconductance (g_m) are increasingly vulnerable to NBTI. Therefore, it is important to examine the NBTI characteristic of a modern device [1-3]. A previous study shows the kinetics of trap generation during NBTI stress by considering the generation of interface trap, bulk trap, and hole traps in preexisting bulk traps [4-6]. The generation of interface trap is presented by using H-H_2 reaction–diffusion (RD) at multi-stage configuration (MSC) based on the 14-nm node FinFET experimental data. The process dependent parameters, such as field acceleration factor (Γ_0) and pre-factor (k_{FIT}), are used to match the experimental data with the simulation result, and it is well matched. However, the temperature dependent parameters are still required to reflect the scattering

mechanism. In the study, the pre-factors are remodeled by considering the temperature dependent scattering rate. Additionally, the trap components are extracted from the experimental data, and multi-V_T of 10-nm node FinFET is also investigated. In addition to FinFET, gate-all-around nanoplate-FET (NPFET) is considered as the next generation device because it enhances the device performance and also completely controls short-channel effects (SCE) [7-10]. This is because the stacking NPFET structure essentially exhibits a higher effective channel width than that of nanowire-FET and FinFET at the same area of gate metal and silicon channel [11]. Thus, the NBTI characteristic of NPFET is also investigated based on the 10-nm node FinFET framework.

3.2 Modeling of NBTI Framework

3.2.1 Device setup

The NBTI characteristic is analyzed using 3D technology computer-aided design (TCAD) simulation. The 10–nm node FinFET is designed based on the International Transistor Roadmap for Semiconductor (ITRS) [12]. Fig. 1 shows the designed FinFET structure and its cross-sectional view. The device parameters in Tab. 1 are used by considering ITRS and also the measured I–V curve of the 10-nm node FinFET. In terms of simulation accuracy, the drain current of 10-nm node FinFET was calibrated and is well matched with the experimental data based on the temperature and the different bias conditions (Fig. 2). The physical model for the FinFET device was based on the electrostatics model. The thin-layer mobility model of Lombardi was applied in order to consider quantization effects on mobility at a thickness corresponding to a few nm. The quantization effects include thickness fluctuation scattering, surface roughness, and phonon scattering [13,14]. In addition, the density-gradient model was used to describe quantum confinement, and a thermodynamic model is applied for simulation considering the temperature of the carrier and lattice [14]. By assuming that most of the NBTI experimental data originated from the interface trap(N_{IT}), the measured NBTI data was calibrated via double interface H–H_2 reaction–diffusion (RD) model for ΔV_{IT} [4,15] and is explained in section III. Additionally, the empirical–stretched exponential models for ΔV_{HT} and ΔV_{OT} were applied into the study.

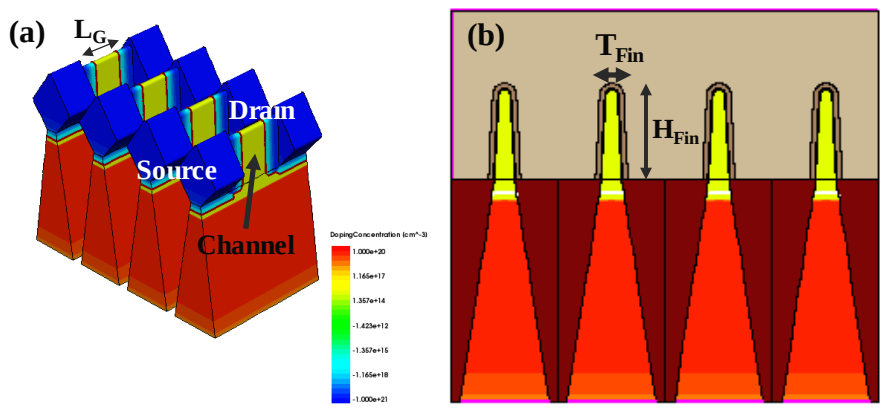


Fig. 1. (a) 3D view of FinFET (b) Cross-sectional view of FinFET

TABLE I
DEVICE PARAMETERS OF FINFET FOR SIMULATION

Device Parameter		Device Parameter	
Channel Length (L_{CH})	18 nm	Fin Height (H_{Fin})	40 nm
Gate Length (L_G)	20 nm	Fin Thickness (T_{Fin})	7 nm
Spacer Length (L_{SP})	15 nm	Effective Oxide Thickness	0.9 nm (HfO_2/SiO_2 : 2.3/0.5 nm)
Channel Doping	10^{15} cm^{-3}	Contact Resistivity	3E-9 $\Omega \cdot cm^2$
Bulk S/D Doping	10^{21} cm^{-3}	V_{DD}	0.75 V

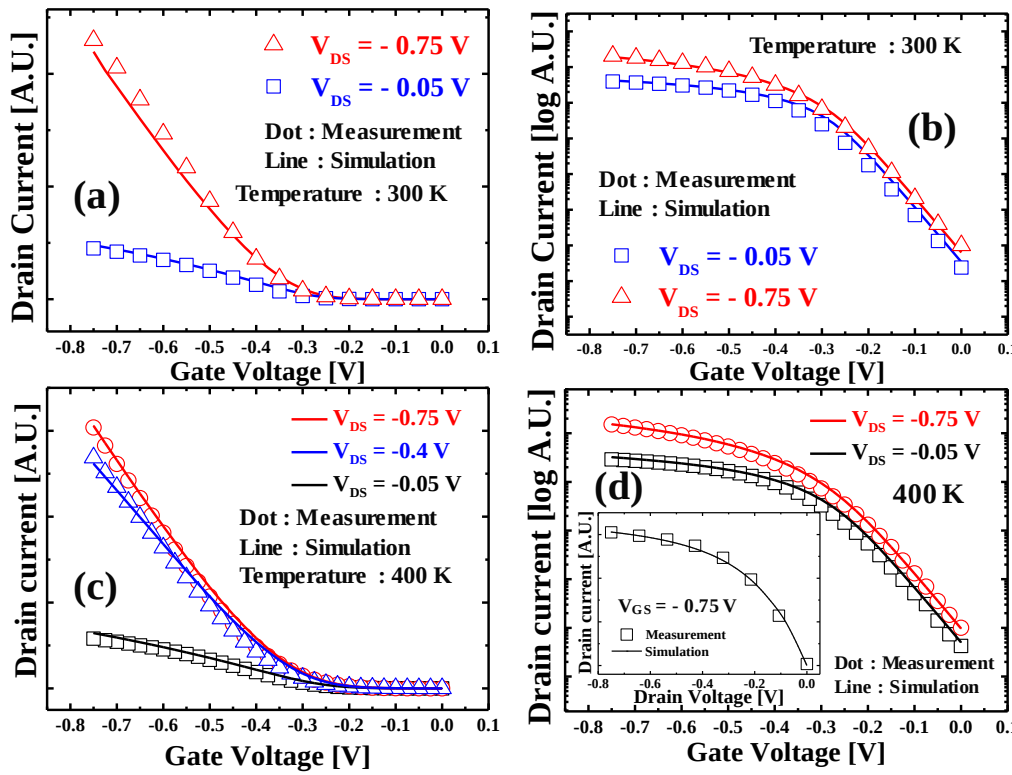


Fig. 2. Calibration of TCAD models with the experimental data of 10-nm node FinFET (a) linear scale of I_{DS}-V_{GS} at 300K (b) log scale of I_{DS}-V_{GS} at 300K (c) linear scale of I_{DS}-V_{GS} at 400K (d) log scale of I_{DS}-V_{GS} and I_{DS}-V_{DS}(inset) at 400K.

3.2.2 Calibration for NBTI Measurement

Fig. 3 shows the double interface H–H_2 reaction–diffusion (RD) model, and it is fully explained in [4-6]. The passivated Si-H bonds at the first interface (Si/SiO) are de-passivated by the inversion layer of a hole. The k_F and k_R parameters denote the forward/reverse reaction rate coefficient composed of each of the chemical reaction activation energy (E_A) and its pre-factors (k_{FIT}, $k_{F0(1)}$, $k_{R0(1)}$, $k_{R0(2)}$). A previous study of [4-6] (as calibrated from the 14-nm process node for FinFET) suggested that the only process dependent parameters correspond to the first interface forward- reaction RD model parameters such as pre-factor (k_{FIT}), field acceleration (Γ_0), bond polarization (α), and temperature activation energy (E_{AF1}). The pre-factor of k_{FIT} is proportional to the capture rate (c), capture cross section (σ) and thermal velocity of hole (v_{th}) [4]. The similar parameter values are used in this paper as shown in Tab. 2. Fig. 4(a) shows the calibrated result of NBTI characteristic for p-FinFET based on the stress gate voltage (V_{GSTR}) at 400 K with the similar Γ_0 reported in [4].

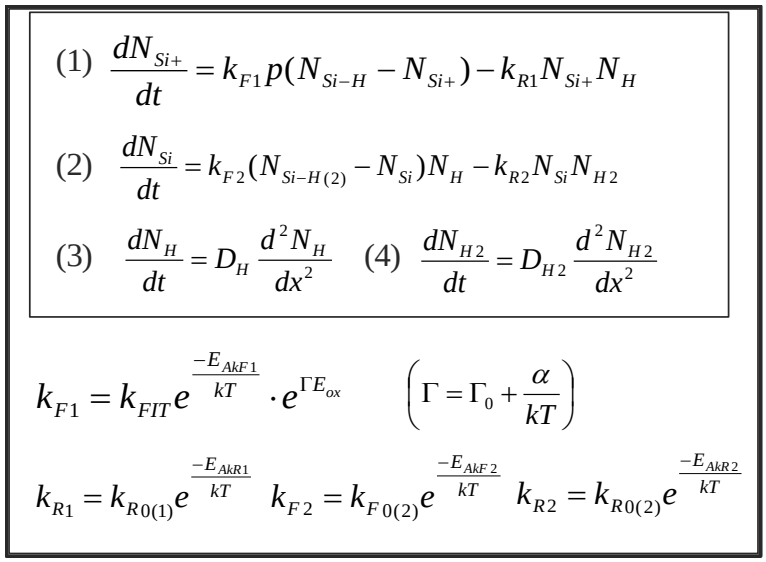


Fig. 3. RD model equations used in this paper. The RD parameters are defined in [4,15] for details.

TABLE II
SIMULATION PARAMETERS FOR R-D MODEL

	[4]	This Work	Unit
k_{FIT}	6e-3	0.8~2.5e-2	[cm³/s]
Γ_0	4e-7	5.5e-7	[cm/V]
α	1.2e-8	1.2e-8	[cm]
E_{AkF1}	0.22	0.22	[eV]
E_{AkR1}	0.12	0.12	[eV]

However, we use the pre-factor of k_{FIT} that is process dependent and temperature dependent. This is because the capture rate (c) and v_{th} depends on the temperature by assuming that capture rate corresponds to the collision between Si-H bond and hole (p). Given that the phonon scattering rate of pure silicon lattice is proportional to $T^{1.5}$ (acoustic phonon) and T^2 (optical phonon) [16], T^{β} denotes the scattering rate based on temperature between Si-H bond and a hole at the interface. Thus, parameter β in Eq. (1) is used by assuming that the interface with Si-H bond is different from the pure silicon lattice. Furthermore, v_{th} is generally proportional to $T^{0.5}$ and $v_{th,300k}$ corresponds to 2.7×10^7 cm/s [17]. Fig. 4(b) inset shows the increased k_{FIT} depending on the temperature (T) with $\beta = 3.5$. The result calibrated with the experimental data is shown in Fig. 4(b) with the temperature dependent k_{FIT}.

$$k_{FIT} = c_0 \cdot \sigma \cdot v_{th} \left(\frac{T}{300K} \right)^{\beta+0.5}$$

$$\left(c_h = c_0 \cdot \left(\frac{T}{300K} \right)^{\beta}, v_{th} = v_{th,300K} \cdot \left(\frac{T}{300K} \right)^{0.5} \right) \quad (1)$$

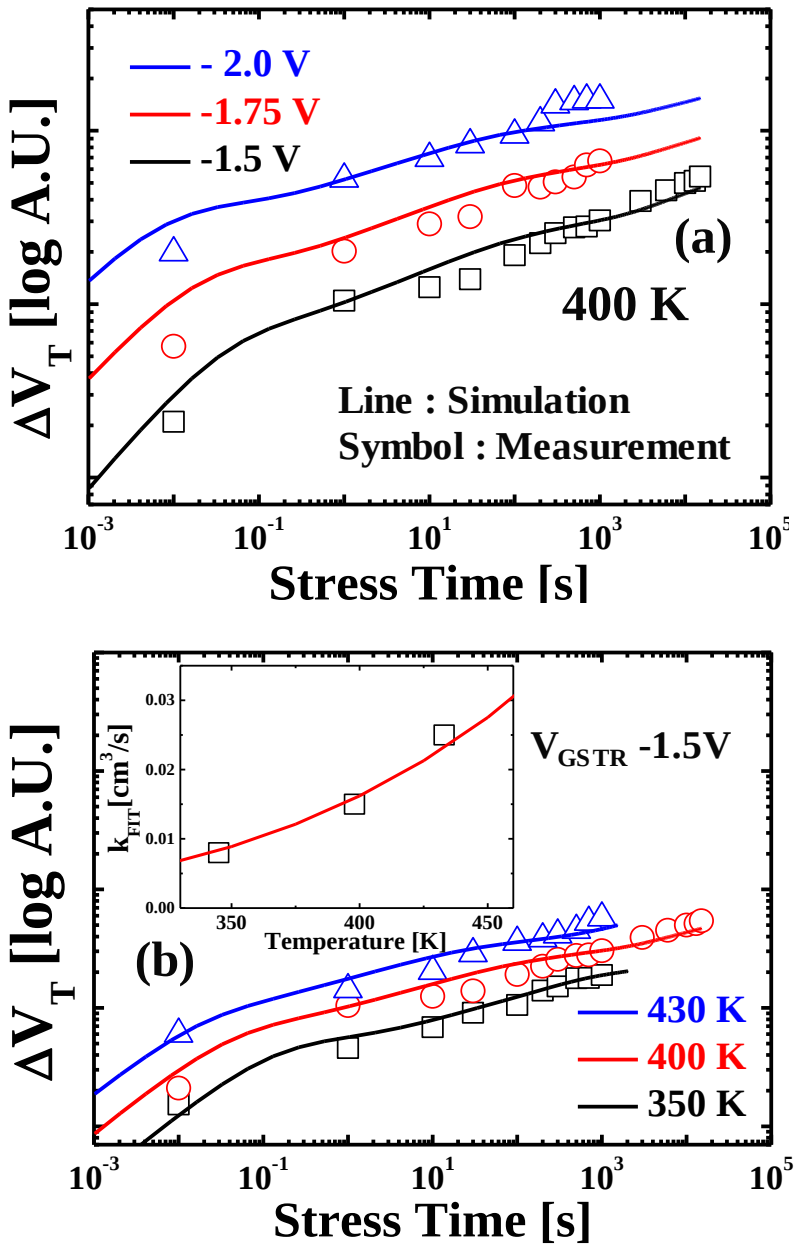


Fig. 4. (a) Time evolution of ΔV_T with the variation of V_{GSTR} (b) Time evolution of ΔV_T with the variation of temperature

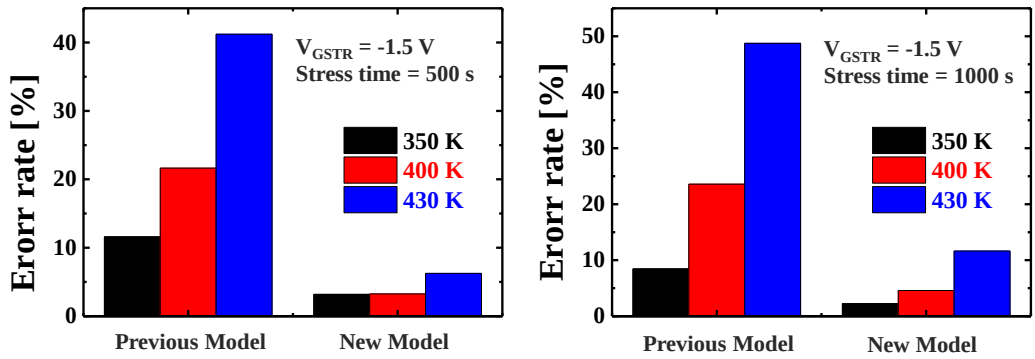


Fig. 5. Comparison of Error rates for previous model and new model
(a) stress time 500 s (b) stress time 1000 s

Fig. 5 shows the comparison of error rates with the measurement for previous model and new model for pre-factor of k_{FIT}. The previous model of k_{FIT} using one constant value significantly increases the error rate with the increase of temperature. In contrast, the newly re-modeled model of k_{FIT} makes the error rate within 10 % even if the temperature changes abruptly.

3.3 Extraction of NBTI Components

The WGFMU measurement is used to obtain the time evolution of $V_{T,}$ and it measures I_D-V_G within 500 μs. Thus, it is assumed that the recovery process during measurement does not occur. Fig. 5(a) shows the raw data from WGFMU. The V_T is obtained at a preset I_{VT}. However, it maintains the previous V_T when the drain current is lower than the preset I_{VT} as shown in Fig. 5(a) inset. Thus, the time evolution of ΔV_T is extracted at 0.1 x I_{VT} in Fig. 5(b). It is observed that two inclinations exist at the high stress voltage of -2.0 V and low temperature of 350 K. This implies that two or more different components exist. The previous study of [4] suggest that it corresponds to N_{IT} with time exponent (n) ~ 0.16 and N_{OT} with n ~ 0.35. Therefore, each component is separately extracted from the measured ΔV_T at V_{GSTR} -2.0 V, 350K (Fig. 6).

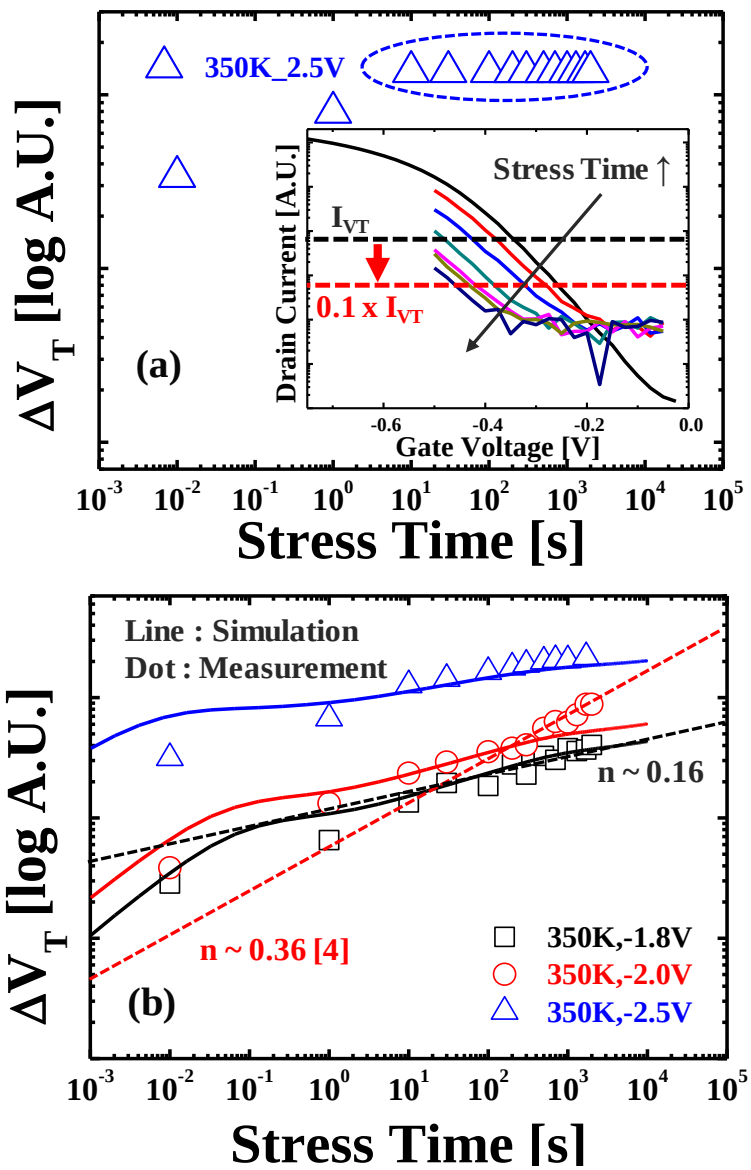


Fig. 5. Time evolution of ΔV_T from (a) the preset of $1xI_{VT}$ and (b) the preset of $0.1xI_{VT}$

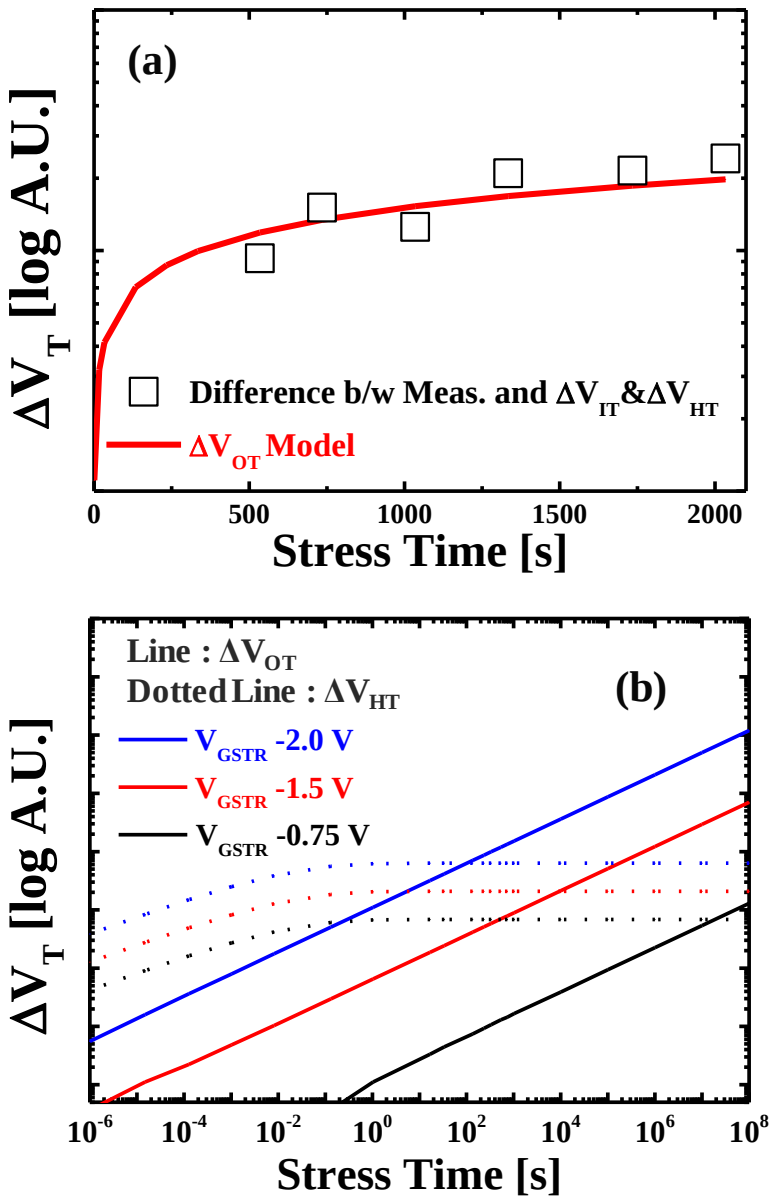


Fig. 6. (a) Time evolution of ΔV_{OT} from extraction (linear scale) (b) Time evolution of ΔV_{OT} and ΔV_{HT} depending on the V_{GSTR}.

Fig. 7 shows the pre-existing hole trap model (V_{HT}) and oxide bulk trap V_{OT} [4]. Specifically, V_{HT} is assumed wherein it is observed at the shortest stress time of approximately 0.01 s. Additionally, V_{OT} is extracted by subtracting V_{IT} from the measured V_T and it matches well with the oxide bulk trap V_{OT} model with $\beta s = 0.36$ (Fig. 6(a)). Each extracted component is shown in Fig. 8. The oxide bulk trap model is based on the time-dependent-dielectric-breakdown (TDDB) model [18]. Thus, ΔV_{OT} abruptly changes based on the V_{GSTR} in contrast to ΔV_{HT} and ΔV_{IT} as shown in Fig. 6(b). Therefore, high stress voltage of V_{GSTR} can overestimate the ΔV_{OT} when it is considered that the real device is operated at a V_{GS} lower than V_{GSTR}. Fig. 9 shows a prediction of overall portion for each component based on the V_{GSTR} by using the stretched exponential model. At a V_{GSTR} corresponding to -2.0 V (as shown in Fig.9(a)), V_{OT} is considered as the most major component. However, a completely different aspect is shown in Fig.9(c). Specifically, V_{IT} is the most significant factor under the operated bias condition ($V_{GSTR}=V_{DD}$). This is because the low V_{GSTR} of V_{DD} does not significantly affect V_{OT} and it corresponds to an almost negligible component. Therefore, the suitable V_{GSTR} is requested to properly predict the end-of-life (EOL) time of device.

Pre-existing trap V_{HT} model	**Oxide bulk trap V_{OT} model**
$\Delta V_{HT}(t) = \Delta V_{HT,\max}\left(1 - e^{-\left(\frac{t}{\tau_{HT}}\right)^{\beta_{HT}}}\right)$ $\Delta V_{HT,\max} = \frac{q}{C_{ox}} k_{NHT} \cdot e^{\Gamma_{OT} E_{ox}} e^{-\frac{E_{AHT}}{kT}}$	$\Delta V_{OT}(t) = \frac{q}{C_{ox}} k_{FOT}\left(1 - e^{-\left(\frac{t}{m}\right)^{\beta s}}\right)$ $m = \eta \cdot (V_{GSTR})^{-\frac{\Gamma_{OT}}{\beta s}} \cdot \frac{E_{AOT}}{kT\beta s}$

Fig. 7. V_{HT} and V_{OT} model equations from [4-7].

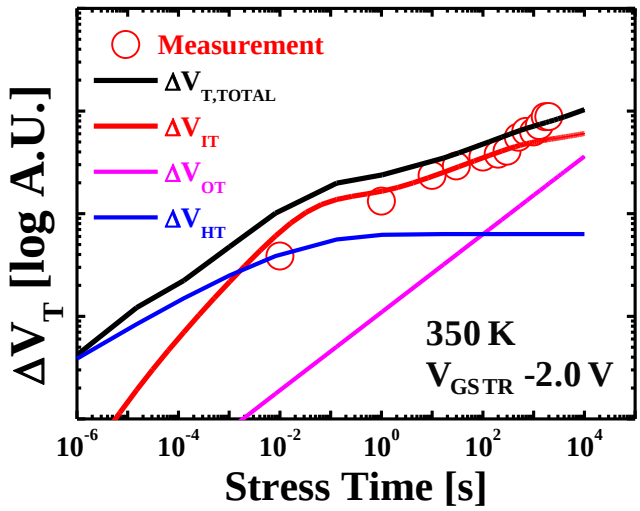


Fig. 8. Time evolution of each trap component from extraction result.

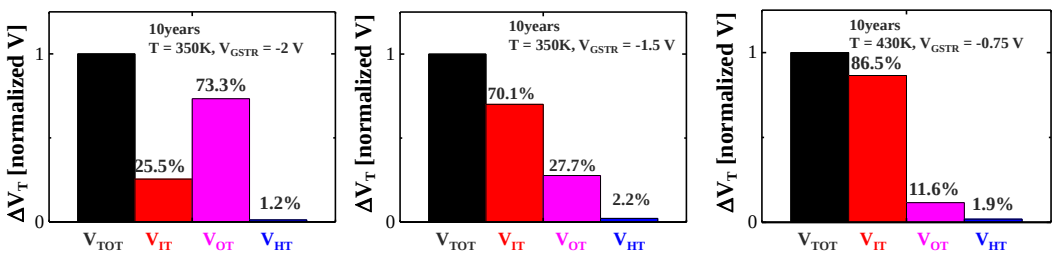


Fig. 9. Overall ΔV_T of each components at a fixed time of 10 years with the change of V_{GSTR} (a) -2 V, (b) -1.5V and (c) -0.75 V

3.4 Analysis of NBTI for Multi-V_T FinFET

Fig. 10(a) shows the simulation result of the time evolution for ΔN_{IT} depending on the V_{GSTR} and gate work-function (WF). It is shown that the same result of ΔN_{IT} is obtained for WF 4.8 eV with V_{GSTR} -1.5 V and WF 5.0 eV with V_{GSTR} -1.3V.

$$\begin{aligned} V_G &= V_{FB} + V_{OX} + \phi_S \\ &= (\Phi_M - \Phi_S) + V_{OX} + \phi_S \end{aligned} \quad (2)$$

$$\Phi_M' = \Phi_M + \alpha \quad (3)$$

$$V_G - \alpha = (\Phi_M - \Phi_S) + V_{OX} + \phi_S \quad (4)$$

Eq. (2) shows the general equation of gate voltage (V_G). Specifically, V_{FB} represents flat-band voltage between gate metal and channel, V_{OX} corresponds to the dropped voltage of oxide, and φs corresponds to the channel surface potential. When the gate work-function (Φ_M) changes, the effective gate stress voltage is also modulated as shown in Eq. (3) and (4). Thus, the same simulation result of ΔN_{IT} is obtained when the change in V_{GSTR} is compensated by the change in WF (Fig. 10(a)). The same effective gate bias is applied to WF 4.8 eV with V_{GSTR} -1.5V, and WF 5.0 eV with V_{GSTR} -1.3 V, and thus the surface potential of the channel and surface electric field and carrier concentration of channel exhibit the same amounts as shown in Fig. 10(b)~(d).

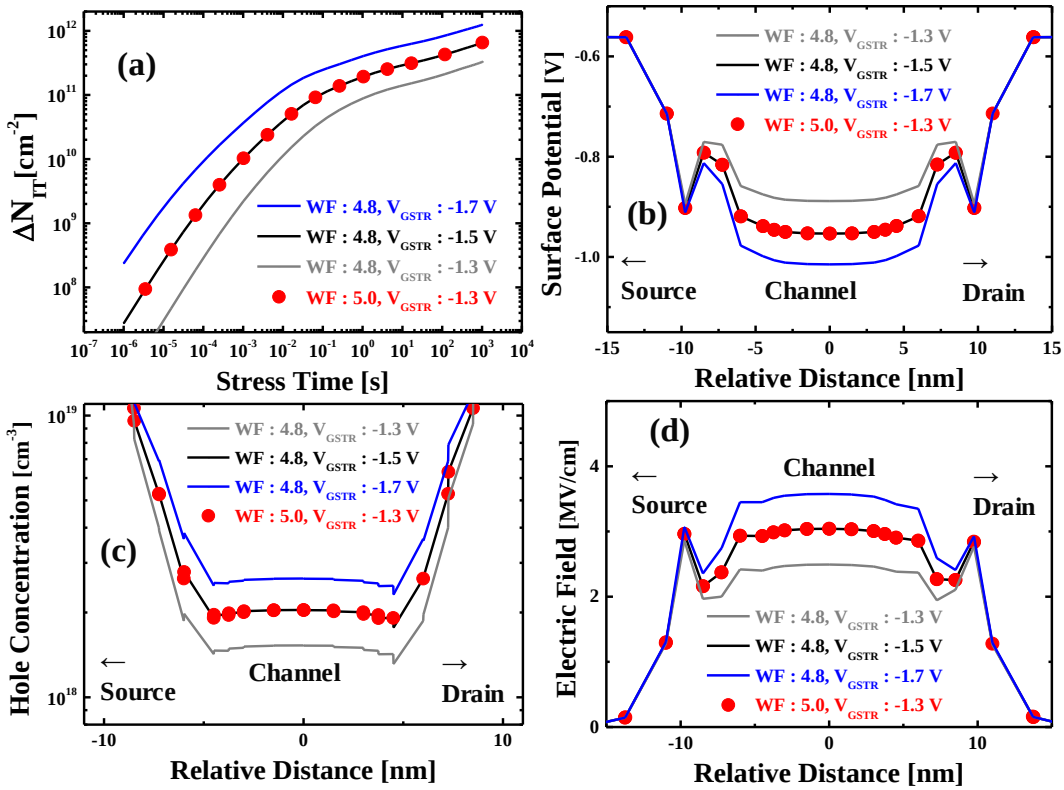


Fig. 10. (a) Generated ΔN_{IT} from NBTI simulation (b) Surface potential (c) Hole concentration (d) Electric Field concentration along the channel direction depending on the workfunction (WF) and V_{GSTR}.

Fig. 11 shows the measured time evolution of V_T for 10-nm-node multi-V_T FinFET. From LVT to HVT, there is an approximate 0.1 V difference in V_T. Each is measured from 10 EA samples, and Fig. 11 shows their average. First, the time evolution of 10 samples of HVT is measured, and their average and the average of $V_{T,HVT}$ is obtained as shown in Fig. 11 and Fig. 12(b). Each sample exhibits process variation in terms of V_T, and thus the I-V curve of each sample for LVT and MVT is measured before applying V_{GSTR}. By assuming that the difference in V_T of each sample is due to gate metal work-function variation, each sample is applied with different V_{GSTR} corresponding to the difference in V_T. The experimental results indicate that, the same amount of ΔV_T is obtained irrespective of multi-V_T in Fig. 11. Therefore, the findings indicate that the process variation of V_T does not affect the generation of traps. In addition, it is noted that not only V_{GSTR} but also the WF is significant factor to determine the device lifetime. Fig. 12(a) shows the average of 10 samples for multi-V_T from LVT to HVT. The WF is tuned as shown in Fig.12(b), and thus it is easily calibrated and well matched with experimental data.

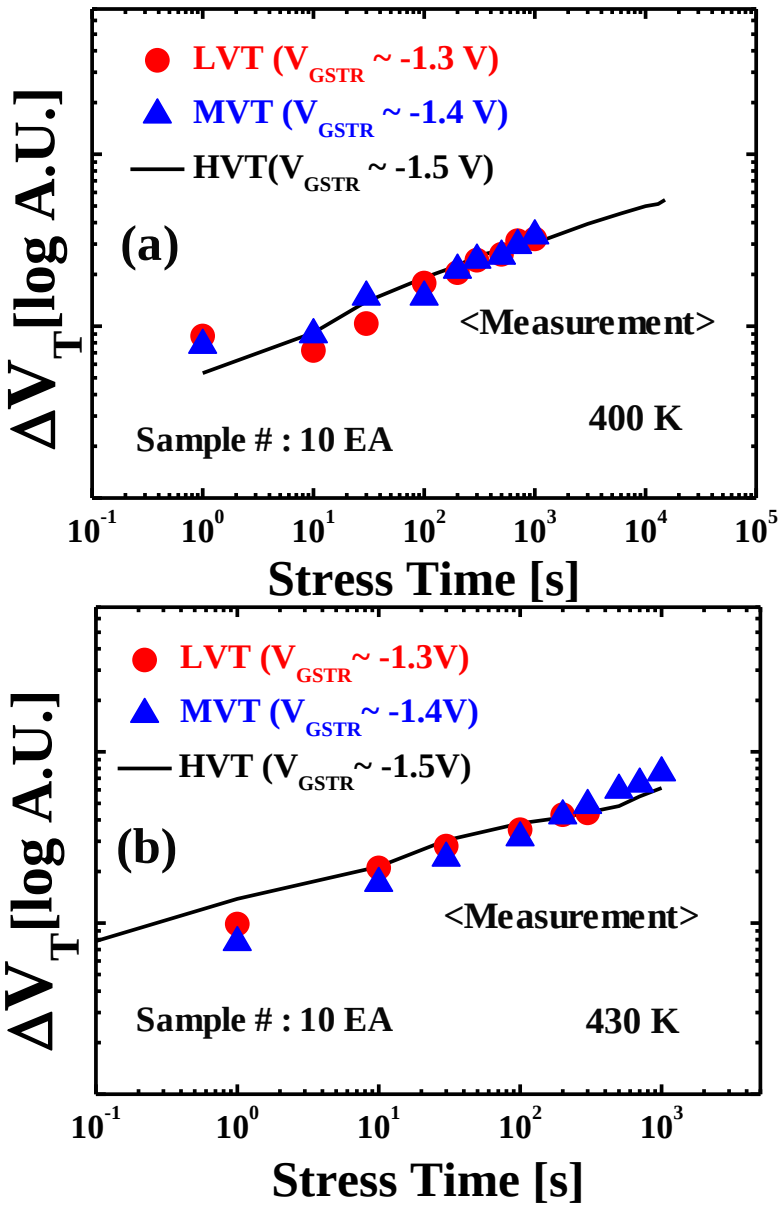
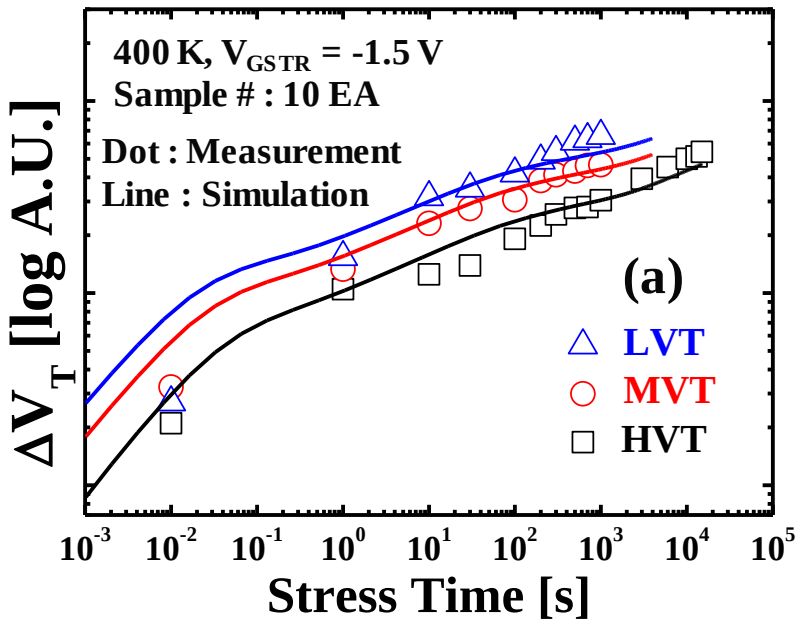


Fig. 11. Time evolution of ΔV_T by compensating WF difference with V_{GSTR} at (a)T=400K (b) T=430 K



(b)	Average V_T (400 K)	Simulation WF
HVT	~ 0.3 V	~ 4.7 eV
MVT	~ 0.2 V	~ 4.8 eV
LVT	~ 0.1 V	~ 4.9 eV

Fig. 12. (a) Time evolution of ΔV_T of Multi-V_T FinFET (b) used simulation WF and average V_T of 10 samples.

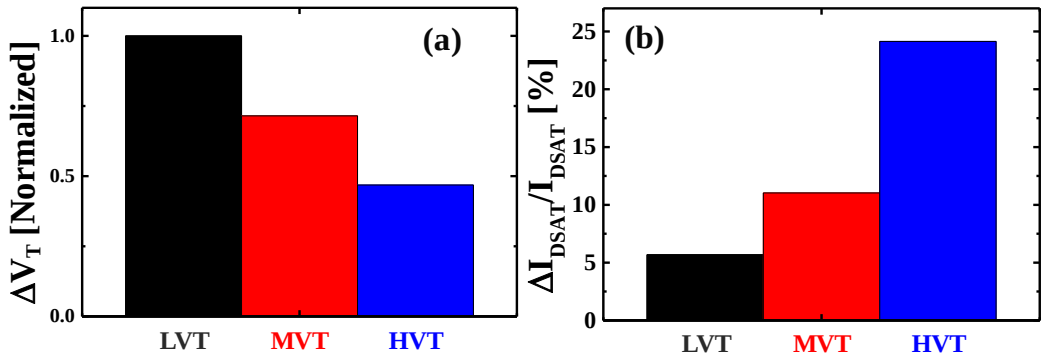


Fig. 13. (a) Overall ΔV_T of Multi-V_T FinFET at a fixed time of 10 years (b) Degradation rate of I_{DSAT} depending on the Multi-VT at a fixed time of 10 years.

Fig. 13 shows the normalized ΔV_T and the degraded $\Delta I_{DSAT}/I_{DSAT}$ depending on the multi-V_T FinFET. The LVT has the larger ΔV_T than that of HVT since it has the larger effective V_{GSTR} as shown in Eq. (4). However, the degraded rate of I_{DSAT} ($\Delta I_{DSAT}/ I_{DSAT}$) presents the different trend of ΔV_T. This is because the initial I_{DSAT} of LVT is much larger than that of HVT, even though the ΔV_T of LVT is larger than that of HVT. Therefore, it is note that the LVT has a strong immunity for NBTI in terms of performance.

3.5 Analysis of NBTI for Nanoplate-FET

A 3-stacked nanoplate-FET (NPFET) is constructed using TCAD simulation tool and it has a 5-nm layer thickness and 45-nm width (Fig. 14). The drain current of the 3-stacked NMOS NPFET is calibrated with [7]. In order to simulate NBTI of PMOS, it is assumed that 3-stacked PMOS NPFET exhibits a I_{DS}-V_{GS} curve similar to that of NMOS due to the epitaxial SiGe with a compressive force to the channel (Fig. 14). Thus, a 5-nm layer thickness and 5-nm spacer length are assumed for the simulation to calibrate with the benchmark of [7]. The parameters are obtained from the fabricated NPFET, which exhibits superior electrostatic control. The calibrated supply voltage is set to 0.65 V. The physical parameters used in the simulation are listed in Table. I of ref. [11].

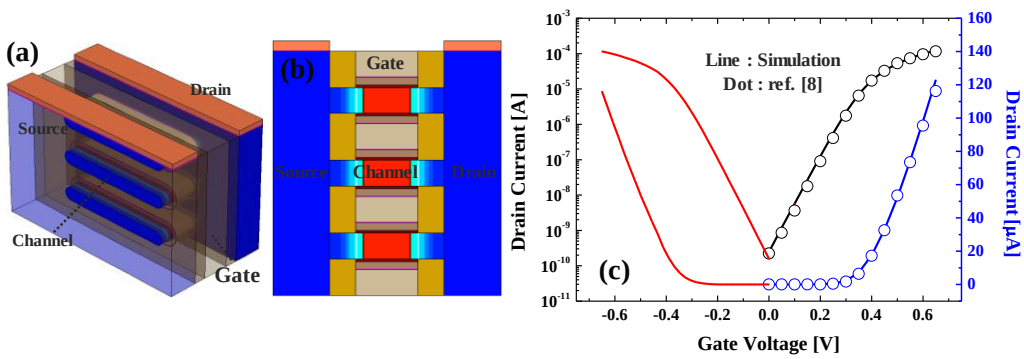


Fig. 14. (a) 3D view of NPFET (b) Cut view of NPFET (c) I_D-V_G of NPFET.

In contrast to the FinFET structure, the highest advantage of NPFET is that it can modulate its structure such as width of NP(W_{NP}) and thickness (T_{NP}). Therefore, the investigation on NP structure is significantly explored [7-11]. Recently, the fabricated NP has two different silicon orientation (Fig. 15(b)). A top-wall of NP has (100) silicon orientation but side-wall of NP has (110) orientation [21]. The (110) orientation of silicon has inherently 1.5 times more surface atom density than that of (100) orientation. Thus, the more Si-H bonds are in sidewall and the more V_T degradation is shown in (100) orientation [20]. Fig. 16 shows the simulation result of the time evolution for ΔN_{IT} with variation in W_{NP} and T_{NP} at V_{GSTR}=-1.7 V, t=1000 s. When the W_{NP} increases, the peak of lateral electric field decreases and the generated N_{IT} decreases as shown in Fig. 16(a) and (b). The trend is also observed with the change in T_{NP} in Fig. 15(c) and (d). However, the decrease in peak electric field is nearly saturated at T_{NP} ~ 8 nm (Fig. 16(c) inset). Additionally, the sidewall of NPFET exhibits the (110) silicon orientation, which exhibits 1.5 times higher surface silicon atom density than that of (100) silicon orientation (topwall) at unit cell [19,20]. Thus, the thicker T_{NP} has the higher initial density of N_{Si-H} and the generation of NIT increases at 10 nm of T_{NP}. This corresponds to an inherent NBTI characteristic of NPFET. Therefore, this can be considered while designing future generations of devices.

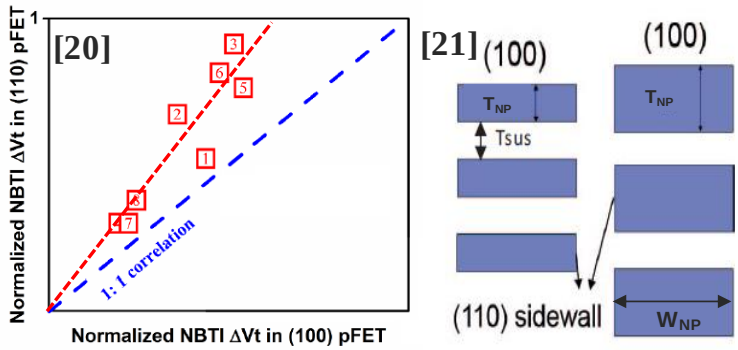


Fig. 15. (a) Normalized NBTI ΔV_T in (100) and (110) PFET (b) Channel cut view of NPFET [20,21]

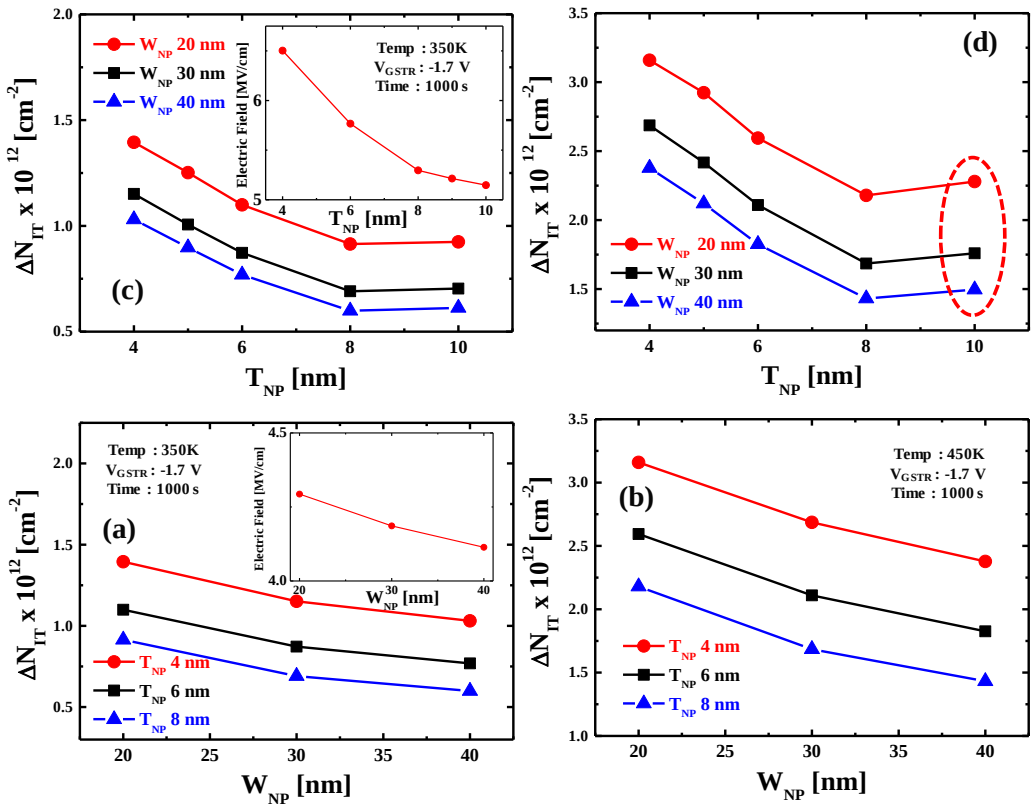


Fig. 16. Generated ΔN_{IT} depending on the W_{NP} (a) T=350K and (b) 450K, Generated ΔN_{IT} depending on the T_{NP} (c) T=350K and (d) 450K.

3.6 Summary

In the study, a 3D TCAD framework of NBTI is used to calibrate the experimental data of 10-nm-node FinFET. A pre-factor from a previous study is remodeled given that the scattering rate is dependent on temperature. The trap components are extracted from experimental data and indicate the excessive stress voltage overestimates the device lifetime. In addition, not only the stress voltage but also the work-function has an effect on the NBTI characteristic from the Multi-V_T experiment. Based on the calibrated simulation framework, the feature of nanoplate-FET is also investigated depending on the structure parameters.

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Chapter 4
Modeling of Parasitic Extension Resistance Considering Spacer Materials

4.1 Introduction

Devices of Gate-all-around gate structures such as nanoplate-field-effect transistors (NPFETs) are considered to be a powerful candidate for sub-5-nm technology nodes due to their strong immunity to short channel effects (SCE) but also their large effective width at relatively small footprint [1-4].

Parasitic resistance and capacitance have been regarded as the main issue since they have a crucial effect on the deterioration of device performance [5]. Spacer engineering, such as dual-*k* spacer and corner spacer, is considered a key technology because it effectively alleviates parasitic components [6-8]. Numerous efforts have been made to achieve parasitic resistance modeling. A previous study [9], derived a comprehensive parasitic resistance model that can be applied to the 3D FinFET. The study [10] also introduced a parasitic resistance model with a hexagonal-shaped raised source and drain (S/D) structure, and considered the accumulation carriers under the gate overlap. In addition, an extension resistance of the BSIM parasitic resistance model was designed considering the accumulation carriers using the S/D flat-band voltage [11]. However, the

previous models do not consider the spacer material and its impacts on parasitic resistance. As the dielectric constant of the spacer material increases, the gate fringing-field induced in the extension region increases. Thus, more carriers accumulate at the extension surface which results in a change in extension resistance [6,12,13]. In this study, the parasitic extension resistance model for NPFET is newly derived considering the spacer material's effect on parasitic extension resistance.

4.2 Carrier Concentration and Mobility

4.2.1 Simulation Setup

Using 3D technology computer-aided design (TCAD) simulation, we analyzed the extension resistance of NPFET (with dimensions as shown in Fig. 1). The NPFET was designed with the goal of the final fabricated device having a 44-nm contacted poly pitch (CPP). Using the results presented in [1] as a benchmark, 5-nm nanoplate layer and identical spacer thickness were assumed for the simulation. In terms of simulation accuracy, the drain current from a three stacked NPFET was calibrated [14]. The gate metal work function was set to adjust the requisite threshold voltage (V_T) to 205 mV [I_{VT} = 100 nA· (W/L)]. The parameters used in the simulation are shown in Tab. 1. The physical model for the extension resistance was based on the electrostatics model. Thus, the simulation was simplified to exclude the quantum mechanical model, the interface trap model, and the stress model. Due to the 5 nm thickness of the NP, electron mobility was degraded due to surface roughness scattering. Thus, the thin-layer mobility model of Lombardi is applied because it takes quantization effects on mobility into account at a thickness of a few nm. These quantization effects include thickness fluctuation scattering, surface roughness, and phonon scattering [15,16]. The series connection of parasitic resistance consists of the contact resistance (R_{CON}) between metal and the bulk S/D, the spreading resistance (R_{SPR}) where the carriers are spread from the narrow extension to

wide bulk S/D, and the extension resistance (R_{EXT}) between the channel and the bulk S/D which possesses a Gaussian doping profile as shown in Fig. 1(b).

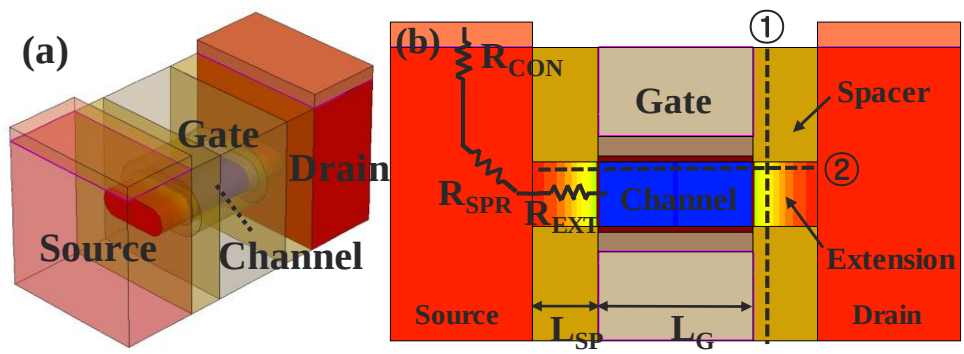

Fig. 1. (a) 3D view of NP FET (b) Cross-sectional view of NP FET and each parasitic component of resistance.

TABLE I
DEVICE PARAMETERS

Device Parameter		Device Parameter	
Channel Length (L_{CH})	12 nm	Contact Resistivity	3E-9 Ω·cm^2
Gate Length (L_G)	12 nm	V_{DD}	0.65 V
Spacer Length (L_{SP})	5 nm	Bulk S/D Doping	10^{18}~10^{20} cm^{-3}
Channel Doping	10^{16} cm^{-3}	Spacer Dielectric	1, 3.9, 7.5, 22
Contacted Poly Pitch	44 nm	Effective Oxide Thickness	0.75 nm (HfO_2/SiO_2 : 1.5/0.5 nm)

4.2.2 Carrier Concentration

As the spacer material varies, only the R_{EXT} varies noticeably because spacer materials with higher dielectric constants induce a denser gate fringing field. It causes the carriers to accumulate at the extension surface region (especially it closed to the gate) and R_{EXT} thus decreases [14]. Given that the bulk S/D is highly doped, other resistance components (R_{CON}, R_{SPR}) are not significantly influenced by the spacer material.

Fig. 2(a) is a cross-sectional view of Fig. 1(b) along the line of ① at $V_{GS} = V_{DD}$. The proposed extension resistance model has a parallel connection between R_{S1} and R_{S2} as shown in Fig. 2(a). R_{S1} has the center area (S_1) assuming that it is independent on the spacer material and it has the carrier concentration as much as Gaussian doping distribution. Generally, a Gaussian doping profile can be expressed as shown in Eq. (1) [10,17] where the L_D is the doping diffusion length and x_{SD} is the end point of the S/D along the channel. N_0 is the bulk S/D doping concentration and N_A is an acceptor concentration (= channel doping concentration for this simulation). The L_D and x_{SD} has the same value of L_{SP} (in Fig. 1(a)) because we assumed that the channel length has the same gate length (L_G).

$$N_{dop}(x) = N_0 \exp\left(-\frac{(x - x_{SD})^2}{L_D^{\,2}}\right) - N_A \qquad (1)$$

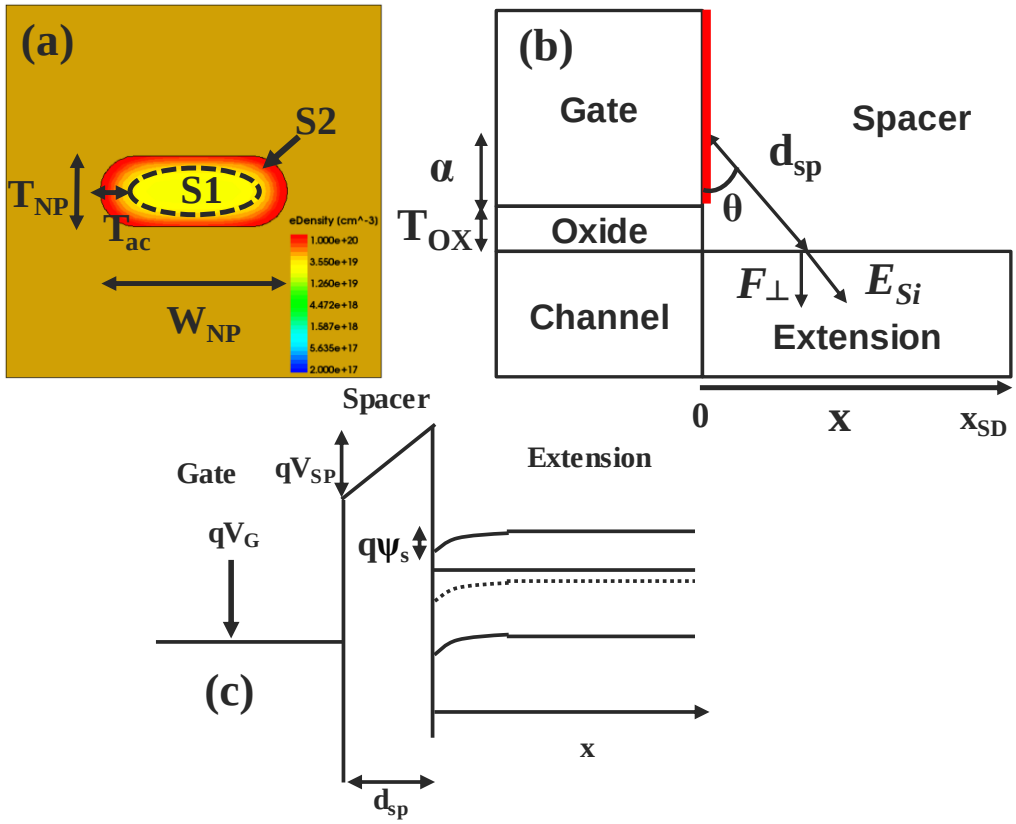

Fig. 2. (a) Cut view of NP and electron concentration (b) Simplified cross section view of 3D NP FET (c) Energy band diagram along the line of d_{sp}

Unlike the R_{S1}, the surface area of R_{S2} has a carrier density which is not limited to the Gaussian doping concentration but also includes the additional accumulated carrier concentration which is dependent on spacer materials. The surface potential of the extension is necessary for the purpose of deriving the additional accumulated carrier concentration formula, which is dependent on the spacer material. In the ideal metal-oxide-semiconductor (MOS) structure (along the line of d_{sp} in Fig.2 (b)), the gate voltage (V_G) drops partly across the spacer insulator and partly across the semiconductor

(extension region) as shown in Fig. 2(c) and Eq. (2). Assuming there is no charge and no carrier in the spacer, Eq. (3) can be derived from Eq. (2) where d_{sp} is the spacer thickness and ε_{si} and ε_{sp} are dielectric constants of silicon and the spacer. It is also assumed that the electric field is perpendicular to both of spacer and silicon with the fitting parameter constant term of α [Fig.2(b)], representing the effective value for different field lines along the x-axis.

(2)

$$\Delta V_G = \Delta \psi_s + \frac{\varepsilon_{si}}{\varepsilon_{sp}} d_{sp} \Delta \mathrm{E}_{si} \tag{3}$$

In addition, Eq. (4) is obtained by solving Poisson's equation and Eq. (5) is also derived applying Gauss's law to Eq. (4) [18]. As the extension is doped with n-type material and the gate bias is positive, the extension region is in the accumulation mode. Thus, the electron concentration parameter (n(x) in Eq. (4)) becomes the dominant factor and Eq. (5) can be simply expressed to Eq. (6).

$$\frac{d^2\psi}{dx^2} = -\frac{dE}{dx} = -\frac{q}{\varepsilon_{si}}[p(x) - n(x) + N_d{}^+(x) - N_a{}^-(x)] \tag{4}$$

$$E_{si}{}^2 = \frac{2kT}{\varepsilon_{si}} N_d [\frac{n_i{}^2}{N_d{}^2}(e^{-q\psi_s/kt} + \frac{q\psi_s}{kT} - 1) + (e^{q\psi_s/kt} - \frac{q\psi_s}{kT} - 1)] \tag{5}$$

$$\Delta E_{si} \approx \sqrt{\frac{2kTN_d}{\varepsilon_{si}} e^{q\Delta\psi_s/kt}} \tag{6}$$

By applying Eq. (6) to Eq. (3), the equation for the relationship between the surface potential (ψ_s) and the gate voltage can be derived considering the spacer material as shown in Eq. (7). α is a fitting constant assuming the gate surface (in Fig. 2(b) red line) is an equipotential surface and it has a fixed value (0.5 nm for HfO_2 spacer ~ 2 nm for Air spacer).

$$\Delta V_G = \Delta\psi_s + \frac{\varepsilon_{si}}{\varepsilon_{sp}} d_{sp} \sqrt{\frac{2kTN_d}{\varepsilon_{si}} e^{q\Delta\psi_s/kt}} \tag{7}$$

$$d_{sp} = \sqrt{(t_{ox} + \alpha)^2 + x^2}$$

By solving Eq. (7) using MATLAB, the surface potential along the d_{sp} was obtained and was well-matched with the extracted surface potential of the TCAD simulation [Fig. 3].

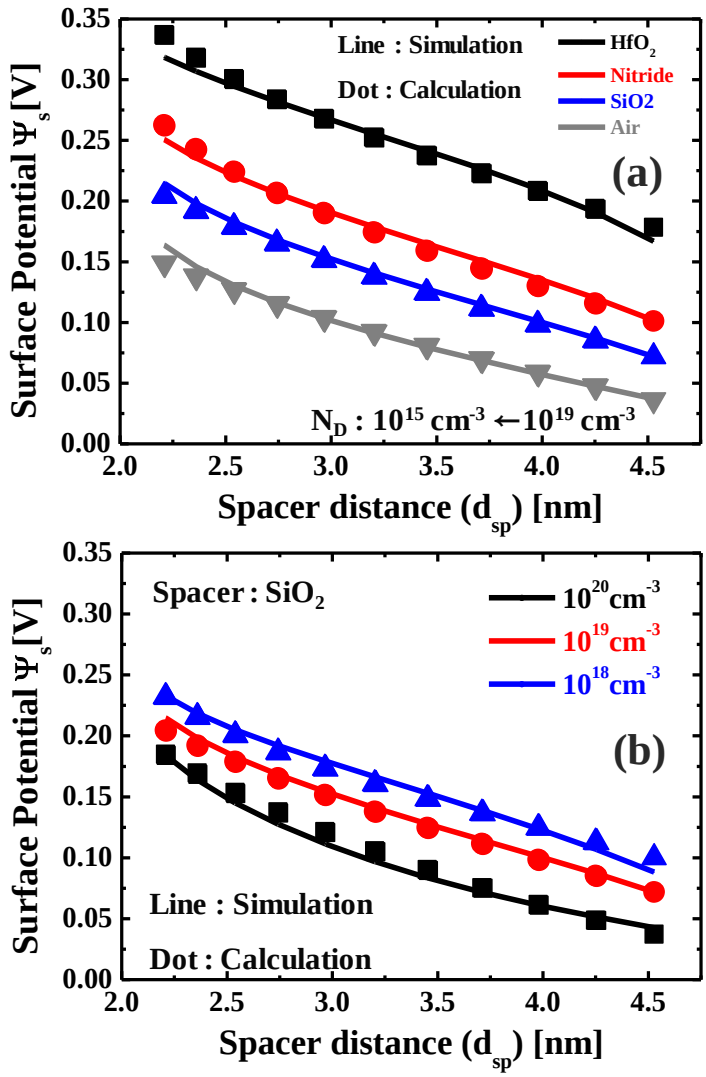

Fig. 3. Surface potential of extension region with the change of (a) spacer materials and (b) bulk S/D doping concentration along the $d_{sp.}$

To derive electron accumulation density at the extension surface, the solved surface potential from Eq. (7) can be applied to the Fermi-Dirac integral function (Eq. (11)). In Eq. (8 and 9), $g_c(E)$ is density of states at energy E in the conduction band and $f(E)$ is Fermi function how many of the existing states at the energy E will be filled with an electron. Boltzmann approximation cannot be applied because the Fermi level (E_F) is not restricted to values $E_F < E_C$-3kT at the accumulation mode. Thus, the general form of the Fermi-Dirac integral is used assuming room temperature (300K) where E_{C0} is the conduction band energy at V_G = 0 V. The Eq. (11) is derived from Eq. (10) using Eq. (2.3), (2.4) and (2.10) from [18].

$$g_c(E) = \frac{m_n^* \sqrt{2m_n^*(E - E_c)}}{\pi^2 \hbar^3} \tag{8}$$

$$f(E) = \frac{1}{1 + e^{(E - E_F)/kT}} \tag{9}$$

$$n = \int_{E_C}^{\infty} g_c(E) f(E) dE \tag{10}$$

$$n = N_C \frac{2}{\sqrt{\pi}} \int_{E_C}^{\infty} \frac{\sqrt{E - (E_{C0} + q\Delta\psi_s)}}{1 + e^{(E - E_F)/kT}} dE \tag{11}$$

where N_C is effective carrier density of conduction band states as shown in Eq. (12).

$$N_C = 2\left[\frac{m_n^* kT}{2\pi\hbar^2}\right]^{3/2} \quad (12)$$

Fig. 4 shows the solved Fermi integral (Eq. (9)) using the obtained surface potential. As the dielectric constant of spacer was changed from Air(ε_{sp}=1) to HfO_2(ε_{sp}=22), the calculated electron density of surface region (in Fig. 1(b) dotted line. 2) was shown to be well-matched with the TCAD simulation. The surface electron density was also well-matched as the bulk S/D doping was changed from 10^{18} cm^{-3} to 10^{20} cm^{-3} as shown in Fig. 4(b).

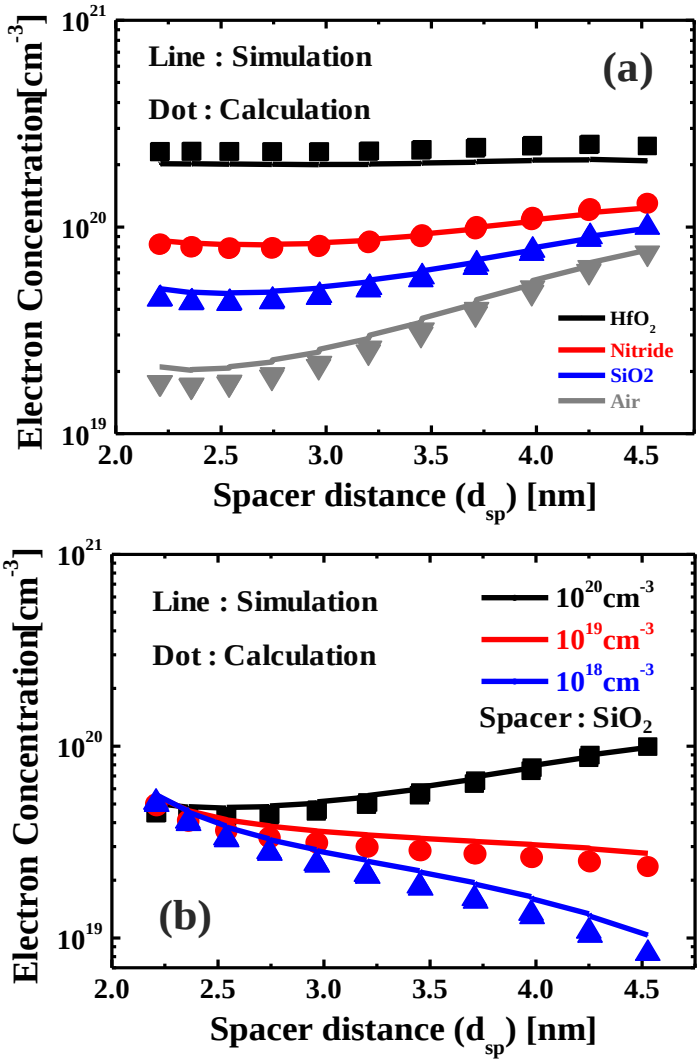

Fig. 4. Electron concentration of extension region with the change of (a) spacer materials and (b) bulk S/D doping concentration along the d_{sp}.

4.2.3 Carrier Mobility

The doping concentration decreased with the Gaussian doping distribution in the extension region from the S/D bulk to the channel direction. In the case of the center electron mobility, it increased gradually towards the channel due to the impurity scattering as shown in Fig. 5(a). This meant that the center electron mobility was unaffected by the spacer material. Thus, the center electron mobility (μ_{S1}) was modeled using Masetti model (μ_b) in Eq. (11) because impurity scattering was the most important factor acting at the center region [19]. However, the surface electron mobility (μ_{S2}) has a strong relationship with the spacer material, particularly close to the gate. This is because spacer materials with higher dielectric constants induce stronger gate fringing-fields. It further degrades μ_{S2} due to surface roughness scattering, which is a strongly degrading factor at low temperatures and in high electric fields in MOS systems [16]. Reflecting this phenomenon, the surface roughness scattering model (μ_{sr}) and Masetti model (μ_b) were simultaneously used to model μ_{S2} along with using Matthiessen's rule in Eq. (11). D is a damping ratio which means how the surface mobility(μ_{sr}) is dominant to the overall mobility depending on the T_{ac} ($D = \exp(-T_{ac}/l_{crit})$, where $l_{crit} = 10^{-6}$ cm) [20]. The T_{ac} is the fitting constant parameter to adjust the extension resistance representing the surface accumulation layer thickness (Fig.2(a)).

$$\mu_b = \mu_{\min 1} + \frac{\mu_{const} - \mu_{\min 2}}{1 + (N_{dop} / C_r)^{\alpha}} - \frac{\mu_1}{1 + (C_s / N_{dop})^{\beta}} \tag{13}$$

$$\frac{1}{\mu_{S2}} = \frac{1}{\mu_b} + \frac{D}{\mu_{sr}} \tag{14}$$

$$\mu_{sr} = \left(\frac{(F_{\perp} / F_{REF})^2}{\delta} + \frac{(F_{\perp})^3}{\eta} \right)^{-1} \tag{15}$$

The Eq. (12) is generally-used surface roughness scattering Lombardi model. F_{REF}, δ, and η are constant parameters having 1V/cm, 5.82x10^{14} cm^2/Vs, and 5.82x10^{30} $V^2cm^{-1}s^{-1}$ respectively [16,20].

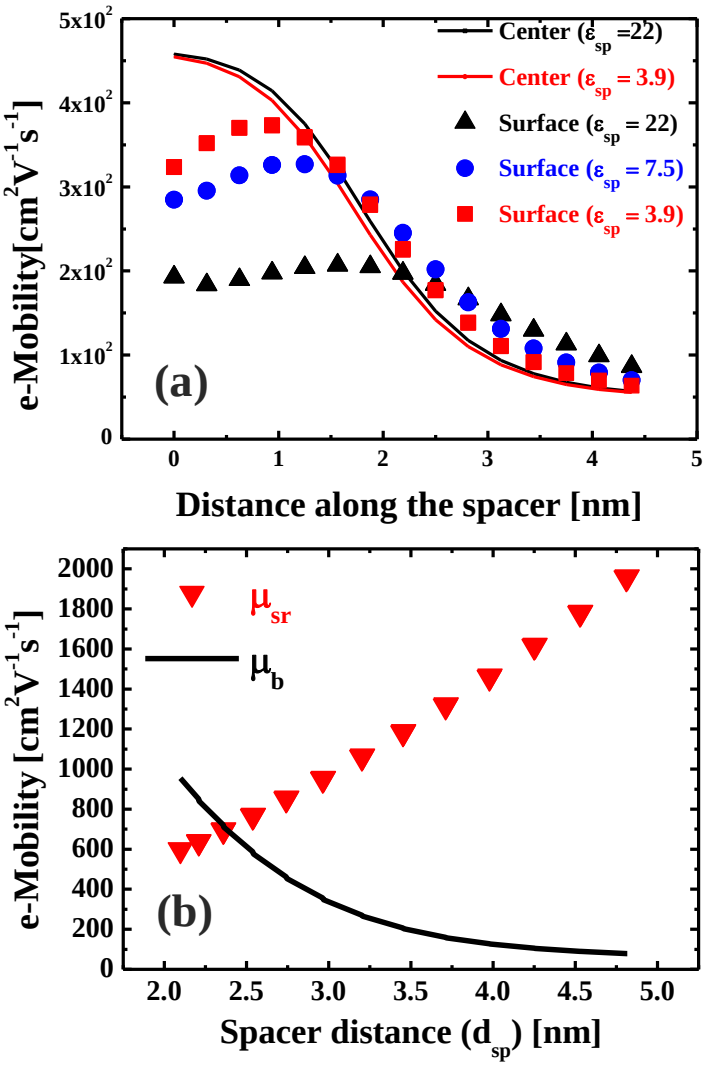

Fig. 5. (a) Electron mobility of the extension region at the surface and the center (b) Electron mobility of $\mu_{b \text{ and }} \mu_{sr}$ along the d_{sp}.

It is necessary to derive the surface normal electric field in order to apply the μ_{sr} of μ_{s2}. As shown in Fig. 2(b), the surface normal field can simply be obtained using the equivalent angle (θ) and the fitting constant α. Using the above equations (12,13), the surface electron mobility was calculated and verified by comparison with the extracted surface mobility from TCAD. As presented in Fig. 6, the calculated surface mobility was very similar to the extracted TCAD mobility when both the dielectric constant of spacer and the bulk S/D doping concentration were changed.

$$F_{\perp} = \Delta E_{si} \cos\theta = \frac{\varepsilon_{sp}(\Delta V_G - \Delta\psi_s)}{\varepsilon_{si} \cdot d_{sp}} \cos\theta \qquad (16)$$

$$(\cos\theta = \frac{T_{OX} + \alpha}{d_{sp}})$$

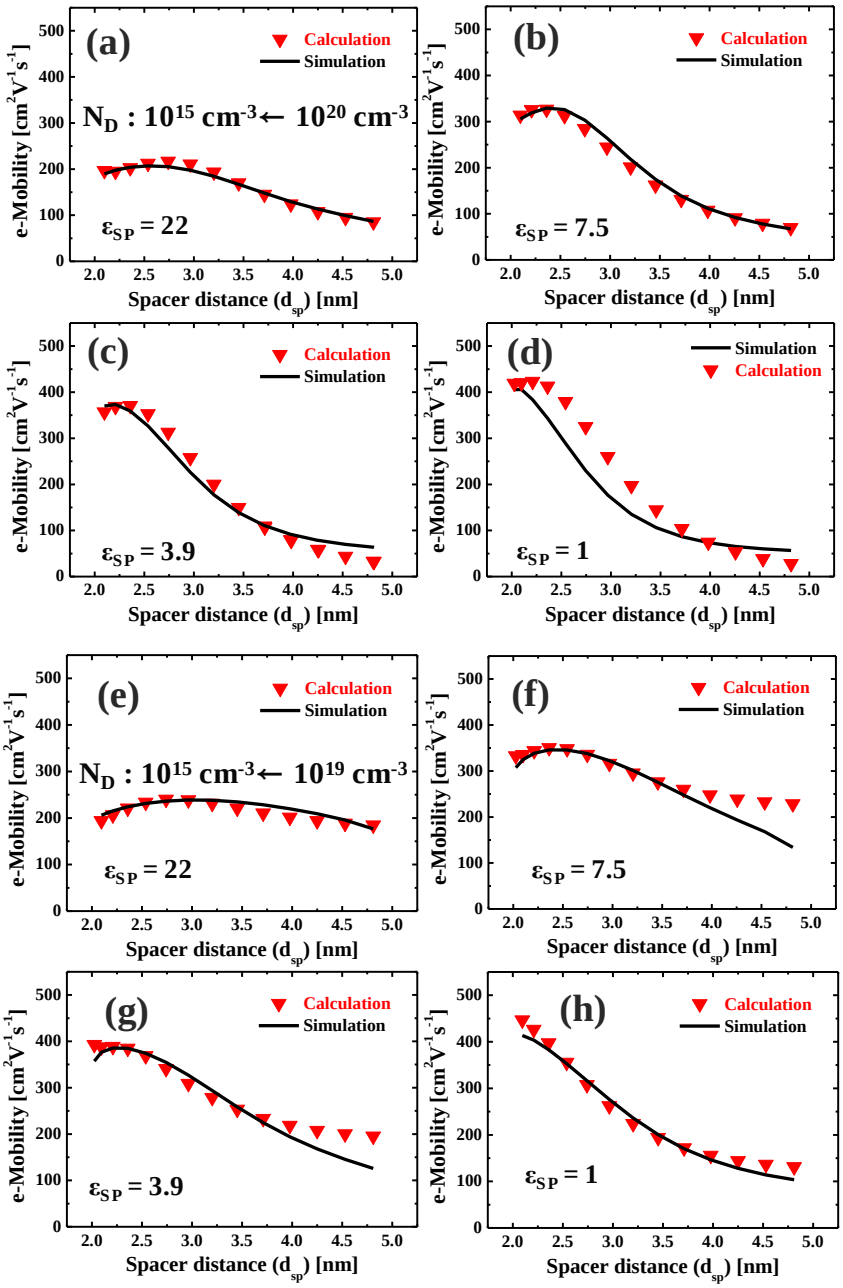

Fig. 6. Electron mobility with the alteration of the spacer materials and bulk S/D doping concentration (10^{20}cm^{-3}: (a-d), 10^{19} cm^{-3}: (e-h)).

4.3 Extension Resistance

In general, the resistance is expressed as the product of Length/Area and 1/conductivity. The conductivity is the product of mobile carrier concentration and the carrier's mobility. Following the above assumption that the accumulated carrier only exists in the S_2 area, each area of S_1 and S_2 is defined in Eq. (14-16). The S_2 area is easily obtained by the difference between the total silicon area (S_T) and the S_1 area. As the extension is separated into the accumulation area (S_2) and the center area (S_1), the total extension resistance (R_{EXT}) can be represented as follows:

$$S_T = T_{NP}(W_{NP} - T_{NP}) + \pi(T_{NP}/2)^2 \tag{17}$$

$$S_1 = ((W_{NP} - T_{NP}) \times (T_{NP} - 2T_{ac})) + \frac{\pi(T_{NP} - 2T_{ac})^2}{4} \tag{18}$$

$$S_2 = S_T - S_1 \tag{19}$$

$$R_{EXT} = R_{S1} \| R_{S2} = \frac{R_{S1} \cdot R_{S2}}{R_{S1} + R_{S2}} \tag{20}$$

$$R_{S1} = \frac{L_{EXT}}{S_1} \left(\frac{1}{q\Lambda(x_1, x_2)} \right) \tag{21}$$

$$R_{S2} = \frac{L_{EXT}}{S_2}\left(\frac{1}{q\Gamma(x_1, x_2)}\right) \tag{22}$$

where Λ and Γ given by

$$\Lambda(x_1, x_2) = \frac{\int_{x_1}^{x_2} N_{dop} \cdot \mu_b(N_{dop}(x))}{x_2 - x_1} \tag{23}$$

$$\Gamma(x_1, x_2) = \frac{\int_{x_1}^{x_2} n(\psi_s(\varepsilon_{sp})) \cdot \mu_{S2}(F_{\perp}(\psi_s(\varepsilon_{sp})))}{x_2 - x_1} \tag{24}$$

In both Eq. (23) and (24), x_1 and x_2 represent the gate edge (x=0 in Fig. 2(b)) and the spacer edge (x_{sd} in Fig. 2(b)), respectively. Λ depends only on the doping concentration ($N_{dop}(x)$) in Eq. (1) and the Masetti mobility model is included. However, Γ is dependent on the surface potential which in turn is dependent on the spacer material and it results in change in both the carrier concentration and also the carrier mobility of the surface region.

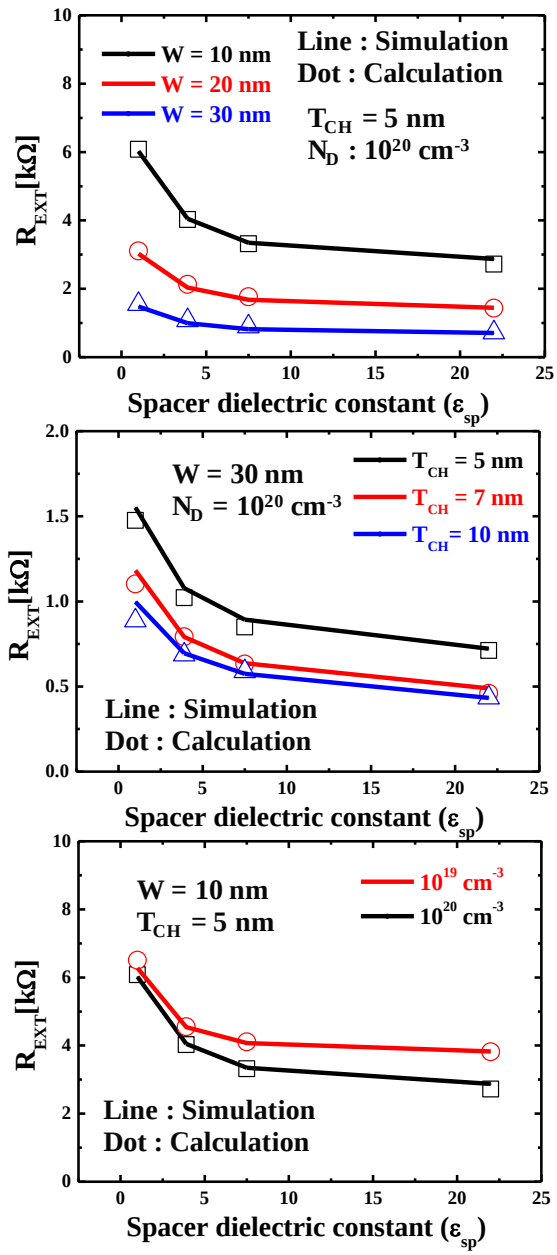

Fig. 7. Comparison of R_{EXT} with the TCAD simulation extraction and the proposed model with the change of (a) NP width (b) NP thickness (c) bulk S/D concentration.

Fig. 7 shows the calculated R_{EXT} using the above equations and the extracted R_{EXT} from the TCAD simulation (R_{EXT} is extracted according to the proposed method of [21]). Spacer materials with higher dielectric constants degraded surface electron mobility (Fig. 5) but simultaneously increased the carrier concentration at the surface. Thus, the overall extension resistance became smaller when materials of higher dielectric constant were used at the spacer region. By changing the various parameters such as nanoplate width, thickness, and S/D bulk doping concentration, the proposed extension resistance error was found to be within 5%. This model can be applicable not only the NPFET but also other device structures and overlap (gate to S/D) region. However, more investigations are still required to apply it to multilayer spacer structure such as dual-k spacer and encased-air spacer.

4.4 Summary

A new model for extension parasitic resistance was proposed considering the effect of the spacer dielectric constant. The newly-proposed model was divided into surface accumulation resistance and center doping gradient resistance, which were connected in parallel. The spacer dielectric constant affected not only the extension surface potential, but also the electric field and it resulted in the alteration of the accumulated carrier concentration as well as the surface roughness scattering. Reflecting this phenomenon in the model, the carrier mobility model as well as the carrier concentration model were newly designed and validated using the TCAD simulation.

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Chapter 5
Conclusion

This dissertation presents the device characteristics of one-digit nanometer nodes which are susceptible to gate electric field focusing on structure comparisons, reliability issues, and parasitic resistance modeling.

In Chapter I, a comparison of GAA nanowire-FETs, NPFETs, and FinFETs was undertaken in the same gate metal and silicon channel areas based on the same condition of parasitic components. It is known that the NPFET structure not only improves the delay performance, but also enhances the immunity to SCEs due to the relatively wide effective channel width. In addition, it was found that the use of a dual-*k* spacer with the NPFET further improves the on-state performances as well as in the off-state which could be a significant solution for devices in future generations.

In Chapter 2, NBTI characteristics were investigated in 10-nm node FinFETs based on experimental data. Considering the scattering rate based on the temperature, the pre-factor of the previous study is remodeled. Additionally, trap components are extracted from experimental data and indicate that the appropriate V_{GSTR} is required in order to properly predict the end-of-life time of the device. Based on the multi-V_T FinFET experimental data, the same amount of ΔV_T was obtained regardless of multi-V_T when the same amount of ΔV_{GSTR} is compensated. Therefore, not only V_{GSTR}, but the WF could also be a

significant factor to determine device lifetime. The NBTI characteristics of NPFETs were also investigated using the calibrated framework of reaction-diffusion and multistate configuration models. In contrast to FinFETs, NPFETs have two different silicon orientations which affect NBTI degradation as the thickness of the NP changes. Thus, they should be considered for device reliability issues.

In Chapter 3, a novel model for parasitic extension resistance was newly proposed considering the gate fringing field which is dependent on the spacer dielectric material. In contrast to the previous model that only explains the accumulation carriers of parasitic resistance by using flat-band voltage, the new model was developed based on the extension surface potential, which is dependent on the spacer dielectric constant. In addition, surface mobility was redefined by considering the change of the surface electric field with respect to the change of the spacer material. The accuracy of the model was validated by changing physical parameters such as nanoplate width, thickness, source and drain bulk doping concentrations, and spacer materials. Also, it was found that the errors were within 5 % of the 3D technology computer-aided design device simulation results.

The field effect on parasitic resistance and reliability will become stronger as devices are scaled down to even smaller sizes. The above research results were obtained based on the lateral CMOS shapes. In the case of CFETs which have NMOS and PMOS on top of each other, the buried V_{DD}/V_{SS} is newly added on the substrate. Thus, the field directions would become more complicated. An investigations considering these various field directions are needed for future next-generation devices.

초 록

CMOS 소자는 FinFET과 같이 Double gate를 갖는 3D MOSFET 구조로 변모하여 지속된 성능향상 및 소자 축소화를 이룩하며 발전해왔다. 그러나 소자 축소화에 따라 게이트 산화막 두께가 감소하면서, 게이트 전압에 의한 전계 역시 증가하게 된다. 증가된 전계는 채널 및 소스/드레인의 mobile carrier 농도 변화를 초래하고 이로 인해, 소자의 성능을 악화시키는 기생저항과 소자의 신뢰성에 영향을 끼치게 된다. 따라서 본 논문에서는 우선적으로 3D MOSFET의 동일 면적의 게이트 및 실리콘에서 소자 구조에 따른 소자의 특성들을 비교하였고, 소자의 신뢰성 중 가장 중요하게 여겨지는 Negative Bias Temperature Instability(NBTI) 특성을 10-nm node Multi-V_T FinFET과 nanoplate-FET(NPFET)에서 분석하였다. 또한, 게이트 전계가 소스/드레인 사이의 절연체인 spacer 물질에 따라 달라지는 점을 고려하여 게이트 전계에 의한 기생저항 모델링을 연구하였다.

다양한 3D MOSEFT을 비교한 1장에서는 동일한 조건의 기생 저항 및 기생 커패시턴스 조건을 충족시키기 위해, 같은 면적의 메탈과 실리콘 에서 채널의 모양(nanowire-FET/FinFET/NPFET)에 따른 다양한 성능을 분석하였다. NPFET은 같은 면적의 채널에서 다른 소자에 비해 훨씬 더 큰 유효 채널 폭을 갖게 됨에 따라 게이트 커패시턴스의 면적을 증가시키게 된다.

이로 인해, 소자의 성능을 향상시킬 뿐만 아니라 단채널 효과를 효율적으로 억제할 수 있다. 이에 더하여, 단일 물질의 spacer 외에 air gap형태의 dual-k spacer를 NPFET에 적용할 경우 기존의 NPFET보다 더 높은 성능향상을 기대할 수 있으며 이는 향후 미래 소자의 성능 향상을 위한 하나의 solution이 될 수 있다.

NBTI를 연구한 2장에서는 인가되는 게이트 전압에 따라 변하는 V_T를 10 nm node FinFET 측정치에 TCAD 시뮬레이션으로 우선적으로 calibration 하였다. 또한, 캐리어의 산란이 온도에 따라 변한다는 점을 고려하여 NBTI 모델을 remodeling 하였다. 또한, 실제 측정된 데이터를 기반으로 NBTI의 각 trap성분들을 추출하였으며, 소자의 수명을 올바르게 예측하기 위해선 적절한 스트레스 전압(V_{GSTR})이 인가 되어야함을 제시하였다. calibration된 시뮬레이션 framework을 통해 NPFET의 구조에 따른 NBTI의 특징 또한 분석하였다.

기생 저항을 새롭게 모델링한 3장에서는 인가되는 게이트 전압의 전계가 spacer 물질에 따라 채널 옆의 기생 저항 영역에 해당되는 extension 부분의 축적되는 캐리어 농도가 변하는 점을 고려하여 모델링하였다. 기존의 extension 기생저항 모델은 이러한 현상을 gate 전압이 아닌 도핑 농도에 의한 평탄전압(V_{FB})에 대한 fitting 변수를 추가함으로써 모델링하였으나 이는 물리현상을 정확하게 반영하지 못한다는 단점이 있다. 따라서, spacer 물질의

유전율에 따라 변하는 전계를 이용하여 extension 부분의 표면 전압을 우선적으로 모델링하였고, 게이트 전압에 따라 변하는 extension 부분의 캐리어 농도 및 캐리어 이동도를 새롭게 모델링하였다. 새로운 기생저항 모델은 게이트 전압에 의한 물리현상을 정확하게 반영하는데 그 의의가 있다.

주요어 : 3D FETs, FinFETs, Nanoplate-FETs (NPFET), Negative Bias Temperature Instability (NBTI), Spacer, Parasitic Resistance

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